Article can be accessed online at http://www.publishingindia.com

Designing a Half-Adder Circuit with Voltage-Mode and Multiple-Valued Logic, Low Power Consumption and High Speed

Hamidreza Dalili Oskouei*, Hajar Zare Bahramabadi, Asghar Ebrahimi*****

Abstract

This article suggests a Quaternary Voltage-Mode Half-Adder Circuit with high speed and low power and capacity consumption. This quaternary circuit is composed of Max Operator, Min Operator, Level Conversion Operator, and Tsum and T-difference Operators Circuits. All these circuits are static and need no current in steady state. All these operators are integrated for the implementation of Quaternary Half-Adder Circuit. This circuit consists of many transistors, but this adder is faster than binary adders.

This article also implements multi-valued logic that is widely focused by researchers and used for the classification of signals. This logic allows the signals to have binary logic levels or more. The operators and elements used in the structure of these circuits are also described here. The suggested circuits are static and operate in voltage mode. There is no static scattering in these circuits and all these asynchronous circuits can be used in integrated circuits.

Keywords: Adder Circuits, Multiple-Valued Logic, Voltage Mode, Operator Circuits, Signal Classification

1. Introduction

Integrated circuits have been improved from low-speed and simple structures to high-speed and complex systems consisting of numerous electronic circuits. Integrated circuit is nothing but a highly advanced electric circuit. An electric circuit is made of several electric parts such as transistors, resistors, capacitors and diodes connected to each other in various ways. These components show different behaviors. As transistors are reduced in size in electronic circuits and increase in number in area units, the electronic circuits enjoy a remarkably higher speed and as a result, their efficiency and productivity level also changes drastically. Moreover, their ability to save data in the memories within a certain space is also improved. The simplest elements should be used in designing and building logic circuits. In other words, to design logic circuits, they should be shortened in different ways and then, optimal logic circuits can be yielded. Logic circuits can be classified under two categories: combinational circuits and sequential circuits.

Combinational circuits are those in which the output at every moment depends on certain inputs at the same moment. In other words, if the inputs are introduced into the network and they are held enough, and the effects of these inputs reach the outputs based on the circuit, then the output values can only be calculated by the set of input values. These modes of combinational circuits are called circuit behavior. Combinational circuits are known to be the circuits without feedback or without memory. Sequential circuits, on the other hand, are the circuits that yield the output based on the earlier history of the circuit. In other words, to estimate the output values for the circuit, it is not enough to have the circuit inputs at this moment, but the output depends on both current and earlier inputs of the circuit.

2. Statement of the Problem

Multiple-Valued Logic (MVL) has been widely focused by researchers during the last two decades because of

* Shahid Sattari Aeronautical University of science and technology, Tehran, Iran. E-mail: h_oskouei@yahoo.com
** Shahid Sattari University of Aeronautical Engineering of Tehran, Iran. E-mail: zare_hajar@yahoo.com
*** Department of Electronic and Engineering, Islamic Azad University of Bushehr, Iran. E-mail: ebrahimi_as@yahoo.com

some critical features [2, 3]. MVL circuits design covers a wide range from simple operator circuits to computational units. Specifically, quantitative approaches have been developed for to the implementation of adders that apply current mode or mixed voltage-current mode circuits. Although the second approach enjoys several advantages, it suffers from the disadvantage of power (electric-energy) consumption because of constant current flux. On the other hand, the adders that operated in voltage mode had a poorer performance [10]. Watanabe et al suggested semi-dynamic adders which used a charge control technique similar to pre-charge method of binary logic. However, dynamic circuits suffer from the well-known disadvantages of clock race, charge redistribution, etc.

Here, a new quaternary half-adder circuit is introduced that operates at voltage-mode. These circuits are designed as functions that apply the operators described above. These adders are based on MOS technology and they do not show the power consumption at their steady states, although these circuits relatively have too many transistors.

3. The Suggested Method

The significance of multiple-valued logic has been emphasized by many researchers. The circuits with multiple-valued logic and MVL systems do not let the signals to have two-valued logic levels or more. Quaternary logic is a multiple-valued logic in which the logic levels of 0, 1, 2, and 3 are correspondent to voltage levels of 0v, 1v, 2v, 3v. Multiple-variable logic is necessary for solving the problems on binary systems because, as compared to binary digital systems, these circuits have the potential to reduce the size of chip by the implementation of internal connections and functions, using VLSI technology. There are two methods for the implementation of half adder: current mode and voltage mode. Current mode has a low efficiency because of power consumption due to constant current. However, voltage-mode adders do not have the disadvantage of static power dissipation. Moreover, there is a half-adder with charge control technique but it suffers from the disadvantage of clock race.

There are two theories about multiple-valued system:

Binary Theory: This system is principally a binary system, but it consists of interconnections that are multiple-valued.

Multiple-Valued Theory: This system is a multiple-valued system but the elements of the process are binary; therefore, encoder circuit is needed to change the binary logic to quaternary logic. This paper will not discuss on encoders and decoders.

Quaternary half-adders will be introduced here. This study is based on MOS technology and it uses a set of quaternary operators. This set consists of the following operators: Max operators, Min operators, level conversion operators, T-sum and T-difference operators.

All these circuits are static ones and they need no current at steady state. All these operators are integrated for the implementation of quaternary half-adder circuit. This circuit consists of two many transistors. But this adder is faster than binary adders.

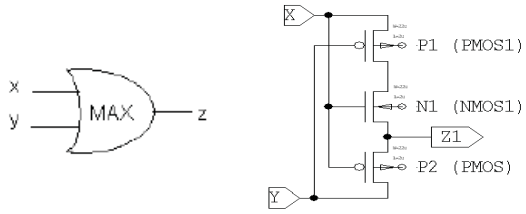
4. Main Concepts (Four Operators)

4.1. Max Operator

Max operator is also called logical addition operator and its output is the maximum value of both inputs.

Figure 4.1: Max Operator and its Array

$$MAX(x,y) = x+y = \begin{cases} x & x > y \\ y & y > x \end{cases} \quad (4\text{-}1)$$

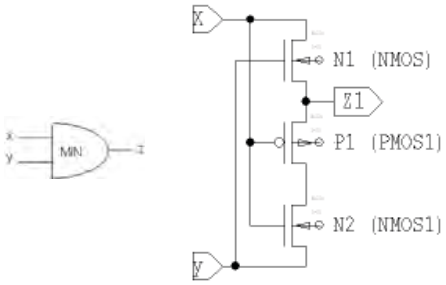


4.2. Min Operator

Min operator is also called logical multiplication operator. The output of this operator is the minimum value of two inputs.

$$MIN(x,y) = x.y = \begin{cases} x & x < y \\ y & y < x \end{cases} \quad (4\text{-}2)$$

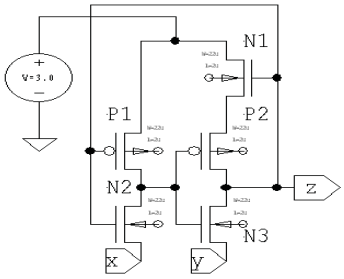
Figure 4.2: Min Operator and its Array



4.3. Level Conversion Operators

There are two level conversion operators: zero level operator and level3 operator. These are semi-lateral operators.

Figure 4.3: Level3 Operator



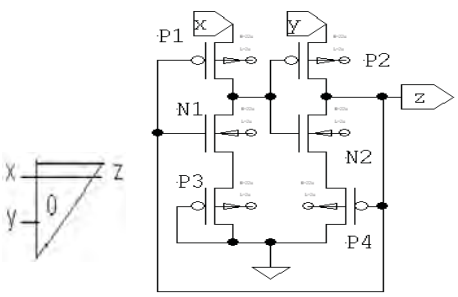
These operators work as follows:

$$a\,x\Big|_{a}^{0} \text{ and } x^{b}\Big|_{b}^{3} \quad (4\text{-}3)$$

$$a\,x\Big|_{a}^{0} = \{0 \text{ if } x \geq a \qquad x^{b}\Big|_{b}^{3} = \{3 \text{ if } x \leq b \quad (4\text{-}4)$$

$$a \text{ if } x < a \qquad b \text{ if } x > b$$

Figure 4.4: Zero Level Operator



4.4. T-sum and T-difference Operators

T-sum operator is also called level-up operator. This operator increases the logic level to the level of (y) sample. T-difference operator is also called level-down operator. This operator decreases the logic level to the level of sample (y). T-sum operator works as follows:

$$X \oplus Y = \min(x+y, 3) \quad (4\text{-}5)$$

$$X \ominus Y = \max(x-y, 0) \quad (4\text{-}6)$$

Figure 4.5: T-sum Operator and its Array

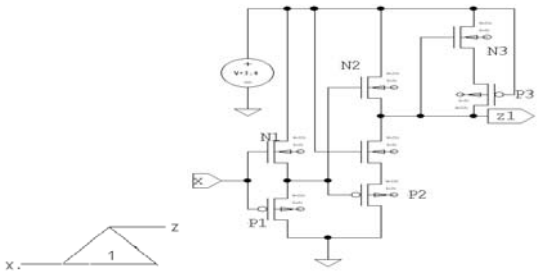
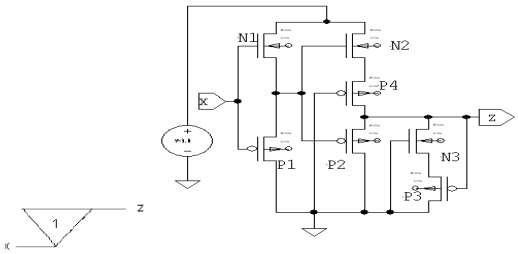


Figure 4.6: T-difference Operator and its Array



4.5. The Suggested Quaternary Half-Adder Encoder Circuit

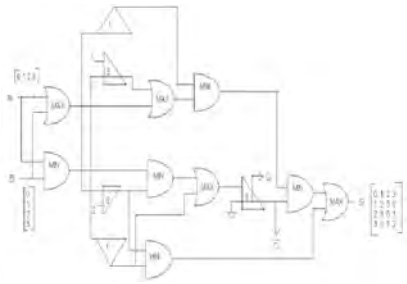
This quaternary half-adder is implemented by a set of operators. 5 max operators, 4 min operators, three level conversion operators and two level-up and level-down operators are used in this half-adder. Operator is used as an internal node to create Carry. To better understand the half-adder function, we apply four inputs of 0, 1, 2 and 3, which are written as a matrix, to two inputs of A and B of the half-adder circuit. The output, complement Carry and Carry are illustrated in table 4-1. So, the sum of two quaternary inputs is obtained in this way and they are shown as a matrix. A total number of 54 transistors

are used in this half-adder. SPICE3 model with 1.5μA technology is used to study this half-adder circuit. The truth table of this quaternary half-adder is illustrated below, where A and B are two inputs and sum and Carry are two outputs. When the circuit reaches the steady state, there is no current from one logic level to another; therefore, there is no static power dissipation. Finally, we have been able to obtain a quaternary half-adder at voltage mode with zero power dissipation.

Table 4.1. Truth Table of Half-Adder for the Sum and Carry

A	B	Sum	Carry
0	0	0	0
0	1	1	0
0	2	2	0
0	3	3	0
1	0	1	0
1	1	2	0
1	2	3	0
1	3	0	3
2	0	2	0
2	1	3	0
2	2	0	3
2	3	1	3
3	0	3	0
3	1	0	3
3	2	1	3
3	3	2	3

Figure 4.7: Voltage-Mode Quaternary Half-Adder



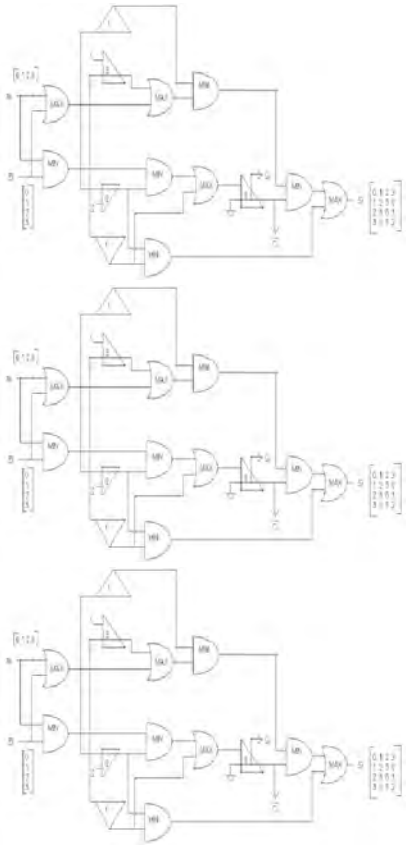
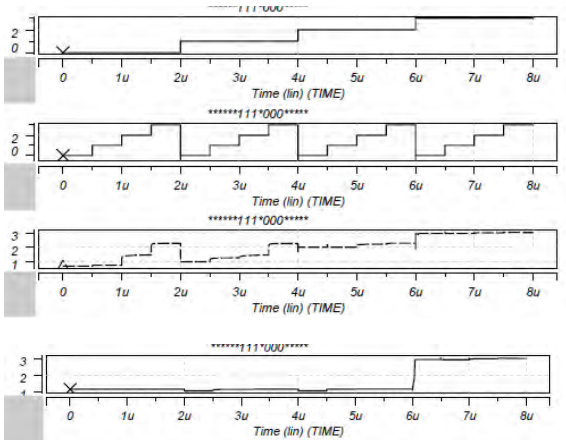
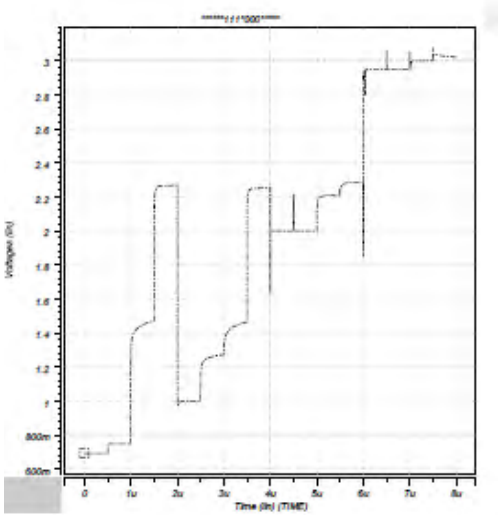


Figure 4.8: Simulation of the Input and Output for the Waveform of Quaternary Half-Adder





4.6. Overall Algorithm for the Suggested Circuit and Description of Its Design and Technical Details

All quaternary operator circuits are used at voltage mode. Just like two-valued logic (0, 1), the quaternary logic also uses continuous electrical changes in order to transmit data as continuous electrical changes from zero to three. Voltages 0, 1, 2 and 3 correspond to the logic values of 0, 1, 2 and 3. Both types of enhancement-mode and depletion-mode of MOFSETs are used in this circuit. The adder is implemented by SPICE2 technology and 1.5µA. Firstly, Max operator is used in the adder circuit in order to calculate the maximum of both inputs. Four Max operators have been used. The second operator used in this circuit is Min operator; 5 Min operators are used. One T-sum operator is used to increase the logic level, and one T-different operator is used to decrease the logic level, and two level conversion operators and are used. Some characteristics of MOS parameter were explained in half-adder design, encoder and decoder. One parameter is threshold voltage. Other parameters include MOS transistor, oxide thickness, surface potential, substrate doping and body threshold voltage. To adjust threshold voltage to the enhancement-mode and depletion-mode transistors, the parameter of body doping is changed. The oxide thickness voltage is kept constant so that it would not affect the threshold voltage. All circuits are simulated by level3 technology and 1.5µA.

$$ {}^{a}x\Big|_{a}^{0} x^{b}\Big|_{b}^{3} $$

For the purpose of simplification, voltage values have been adjusted to the corresponding logic values. That is to say, 0, 1, 2 and 3 volts show 0, 1, 2 and 3 logic surfaces. Both enhancement-mode and depletion-mode MOSFET are used. The performance of the suggested circuits is studied by SPICE in 0.7µm technology [7, 8]. Watanabe suggested a pattern-recognition method for the implementation of MVL function [9, 10]. By this method, the truth table of a function can be considered as an aggregate of the logic-value patterns. This method is specifically explained as follows. The matrices (illustrator of truth tables) are produced by applying the variables to the operators. This step can be repeated again by the variables and matrices obtained before. The next step is recognition of the patterns which are equivalent to the parts of the final matrix (function truth table) in all produced matrices. Finally, function truth table is formed by all matrices in which the patterns have been recognized. The above-mentioned method for building a half-adder are used as functions in the following sections.

The suggested quaternary half-adder is composed as a quaternary function. The operators that were introduced in the earlier study [6] are used for the implementation of the circuit that is shown in figure 1. To better realize the performance of the suggested circuit, the logic levels are presented in the form of a matrix for every node. The construction of circuit based on pattern-production method will be comprehendible if the circuit matrices are considered from right to left. The operator of $x^{b}\Big|_{b}^{3}$ is used with its internal node, as it was defined earlier [8]. We should bear in mind that both signals of carry Ci (where i=0, 1) and complement carry $\bar{C}_i$ are produced and both are used as inputs to the input carry of the quaternary full-adder. Finally, 54 transistors are used for the implementation of the half-adder illustrated in figure 1.

To study the exact function of the half-adder, SPICE simulation is used and the results are shown in figure 2. As it can be observed, when the circuit reaches a steady state, there is no current from one logic surface (i.e. corresponding voltage) to another. The delay at the worst state of the suggested half-adder is 11.3 nsecs for the overall Si and 12.1 nsecs for carry Ci. As a result,

the final circuit is a quaternary static voltage-mode half-adder, with no static power dissipation.

5. Conclusion

Quaternary voltage-mode half-adder circuit is introduced in this article. This circuit has a higher speed, lower consumed power and capacity. The operators and the elements used in these circuits are also explained here. This set of operators consists of Min operator, Max operator, T-sum and T-difference operators, and level conversion operator. These circuits use enhancement-mode and depletion-mode transistors. The suggested circuits are static and operate at voltage mode. There is no static scattering in these circuits and all these circuits can operate in VLSI and they don't need clock. These results show a higher speed and more desirable efficiency for this design compared to other ones.

This article presents a new quaternary static voltage-mode half-adder which does not consume electric energy at steady state performance. It was produced by six operators. This circuit is also faster than binary adder in parallel addition. This circuit performs well at all calculations. All circuits used in this half-adder are asynchronous and do not use clock. Two threshold voltages are used for enhancement-mode and depletion-mode transistors. The consumed power in this article is lower than what was reported in other studies. The circuit speed has also been improved. For a higher efficiency of this circuit, the following solutions are suggested: for better improvement of circuit speed, an analog driver can be used for quaternary voltage-mode circuits. To improve the stability of the circuit, the frequency compensators can be used in the voltage mode quaternary structure. Quaternary circuits can be used in current mode and the result can be compared with the suggested circuit. The occupied area of the chip can be calculated by drawing the circuit's layout and then it can be compared with other studies.

Two control loops are needed in this system. The first loop is the tracking control algorithm for the Max power point based on the calculation of photovoltaic output power and power change that is determined by comparison of current and former voltage levels. To calculate the reference voltage that is used as the set-point voltage for the adjustment of photovoltaic voltage, the second loop adjusts the array voltage to correspond to reference voltage. In this method, P & O (perturb and observe) algorithm is used to track the max power point. However, the array voltage is changed at every control cycle in this method and array voltage fluctuates near optimal operating voltage until it obtains max power point. This leads to power dissipation in the yielded power.

References

1. Madurwar, K. P. & Dakhole, P. K. (2009). *Low Power Quaternary CMOS Circuit Design*. IEEE Transaction on Computers, (pp. 168-172).
2. Thoidis, I. M., Soudris, D., Fernandez, J. M. & Thanailakis, A. (2001). *The Circuit Design of Multiple-Valued Logic Voltage-Mode Adders*. Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium, (4, 162-165).
3. Etiemble, D. & Israel, M. (1998). *Comparison of Binary and Multi-valued IC According to VLSI Criteria.* IEEE Transaction on Computers, (pp. 28-42).
4. Thoidis, I. A. (1998). *Quaternary Voltage-Mode CMOS Circuits for Multiple-Valued Logic*. *IEE Proceedings-Circuits, Devices,* and Systems, *145*, *71-77.*
5. Smith, M. J. S. (1997). *Application-Specific Integrated Circuits*. U.S.A: Addison-Wesley.
6. Thoidis, I., Soudris, D., Karafyllidis, I., Christoforidis, S. & Thanailakis, A. (1998). *Quaternary Voltage-Mode CMOS Circuits for Multiple-Valued Logic*. Circuits, Devices and Systems, IEE Proceedings, 145(2), 71-77.
7. Watanabe, T., Matsumoto. M. & Li, T. (1988). *CMOS Four-Valued Logic Circuits using Charge-Control Technique*. Symposium on Multiple-Valued Logic, (pp. 90-97).
8. Current, K. W. (1994). Current-mode multiple-valued logic circuits. *lEEE Journal of Solid State Circuits*, February, 29(2), 95-107.
9. Jain, A. K., Bolton, R. J., Abd-El- Barr, M. H. (1993). *CMOS Multiple-Valued Logic Design- Part II: Circuit Implementation.* IEEE Transaction on Computers, (pp. 514-522).
10. Thoidis, I. M., Soudris, D., Karafyllidis, I., Christoforidis, S. & Thanailakis, A. (1998). *Quaternary Voltage-Mode CMOS Circuits for Multiple-Valued Logic*. Circuits, devices and systems, IEE Proceedings, 145(2), 71-77.