Design of Fully Differential Telescopic Op-amp with Common Mode Feedback in 0.25µm CMOS Technology

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Abstract

This paper presents an enhanced two stage fully differential op-amp with common mode feedback that achieves improved dc gain, common mode rejection ratio and speed of the op-amp. Two stage op-amp implemented using the telescopic cascode amplifier and common source amplifier. Telescopic operational Op-amp has higher gain, higher pole frequency and lower power dissipation than other configuration and common source amplifier used as transconductance amplifier that help to achieve specification with lower tail current. A high gain, high speed and wide output swing CMOS fully differential operational amplifier is designed using 0.25µm CMOS technology and its various parameters are simulated by using T-Spice. In addition nulling resistor compensation is used to cancel the second pole which is implemented by a MOSFET operating in deep triode region. After the simulation we achieve the Open loop gain ≥80dB, Common mode gain is ≥85dB, Phase margin ≥50o ,Gain bandwidth frequency 200MHz and Output Swing ≥1.2V peak to peak. Finally we conclude that the fully differential Op-amp has many advantages over the single ended counterparts thus it can used in many application like analog to digital convertor, rail to rail design, and other analog IC design.

Keywords: Op-amp, CMOS, Telesccopic cascode Op-amp, open loop gain, CMRR, Compensation.

Introduction

Operational Amplifier are an integral part of many analog and mixed signal system. Op-amps with vastly different level of complexity are used to realize functions ranging from DC bias generation to high speed amplification of filtering. The design of Op-amp continuous to pose a challenge as the supply voltage and transistor channel length scale down with each generation of CMOS technologies. Designing high-performance analog integrated circuits is becoming increasingly exigent with the relentless trend toward reduced supply voltages. At large supply voltages, there is a trade-off among speed, power, and gain, amid other performance parameters. Often these parameters present contradictory choices for the Op-amp architecture. Speed and accuracy are two most important properties of analog circuits, however optimizing circuits for both aspects leads to contradictory demands. The realization of a CMOS Op-amp that combines a considerable dc gain with high unity gain frequency has been a difficult problem. There have been several circuit approaches to evade this problem [4].

Unlike conventional signal-ended op amps, fully differential op-amps have a differential input and produce a differential output. They have some advantages over the signal-ended op amps and are widely used in modern CMOS integrated circuits. For example, by generating "complementary" outputs on both differential arms, fully differential op amps provide roughly twice output swing as their single-ended counterparts. And achieving a large swing becomes more and more important in the modern CMOS circuit design as the supply voltage decreases. Besides, as a balanced circuit with perfectly symmetric components on each side, fully differential op-amps are less susceptible to common-mode noise and even-order nonlinearities. A disadvantage of this topology is that it usually needs a common-mode feedback circuit to control the common-mode output voltage, which increases the design complexity [4] and differential circuits occupy

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twice as much area as single ended alternatives in practices this is a minor drawback [3].

In this report, we discuss the design process of a fully differential Op-amp satisfied certain specifications and show related simulation. Section 2 describes the different parameters of the Op-amp.

DESIGN CONSIDERATION AND TOPOLOGY CHOICE

Topology: Two stage vs. Gain Boosting

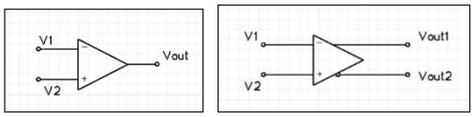
For Op-amp design we need to have knowledge about various topologies and their advantages and disadvantages. Our specification have a high gain (80dB), wide bandwidth (200MHz) and high CMRR (90dB). According to this single stage telescopic or folded cascode can hardly meet the specification. Output swing of single stage telescopic Op-amp are relatively limited and having difficulty in shorting their inputs and outputs. This difficulty can alleviate by using folded cascode Op-amp but at the cost of higher power dissipation, lower voltage gain and lower pole frequencies [1]. For using this two single stage topologies we take the small tail current to boost the gain and implement wide swing cascode configuration to achieve large output swing.

Therefore we choose the two popular topologies first is two stage and second is gain boosting. As compared to gain boosting, two stage topology has a larger output swing, lower power dissipation and input referred noise. Although power and noise is not our primary concern, it always better to have them reduced. So two-stage topology seems more favorable for this particular op amp design. Gain boosting is also possible to achieve larger swing level by using wide swing configuration, but again it is extra power and complexity [5].

Based on these analysis analyses, two-stage topology with first-stage high gain and second-stage high output swing is chosen.

Output Stage: Differential vs. Single-Ended

We have two options for output stage of op-amp one is differential output and second is single ended output. In Single-ended op amps shown in fig.1 (a) have two inputs, a positive and negative input, which are understood to be fully differential. They have a single output, which is referenced to system ground. Schematic symbol for the fully differential Op-amp shown in fig.2 (b) The op amp has two power supply inputs, which are connected to bipolar power supplies (equal and opposite positive and negative potentials), or a single potential, with a positive supply and a ground connected to the power supply pins. These power supply pins are often omitted from the schematic symbol, when power supply connections are implied elsewhere on the schematic [11].



(a) (b)

Fig. 1 (a) Single-Ended Op Amp Schematic Symbol (b) Fully Differential Op Amp Schematic Symbol

Fully differential amplifier have many advantages like increases the output voltage swing and noise immunity, reduces even order harmonics, had large output dynamic range and most important fully differential telescopic op-amp consume less power than fully differential folded cascade op-amp. Hence we choose differential output stage for its simplicity of design and will try to size the tail device as small as possible to avoid overshooting.

SINGLE STAGE TELESCOPIC FULLY DIFFERENTIAL OP-AMP

Cascode configurations may be used to increase the voltage gain of CMOS transistor amplifier stages. This structure has been called a 'telescopic-cascode' op amp because the cascode are connected between the power supplies in series with the transistors in the differential pair, resulting in a structure in which the transistors in each branch are connected along a straight line. The main potential advantage of telescopic cascode op amps is that they can be designed so that the signal variations are entirely handled by the fastest-polarity transistors in a given process [7, 8]. In the first stage, we were simply looking for a configuration that allowed for high gain, low noise and minimal current since output swing is less critical. The folded cascode and the telescopic configurations were considered since we required at least one cascoded stage for a gain on the order of $\left(g_{mr_0}\right)^2$.

A high swing configuration still needs to be used to insure that all the devices in this stage are in saturation. In comparing the two topologies, the folded cascode has more current legs and more devices in the signal path. This leads to larger static current and more noise contributors [17].

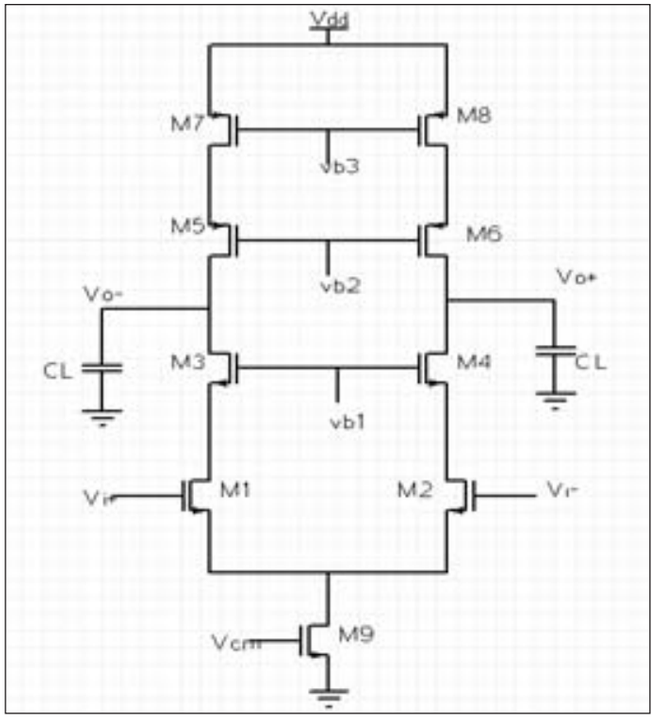


Fig. 2 Telescopic Differential Amplifier

On the other hand, the telescopic configuration has half as many current legs and fewer devices. A telescopic cascode op-amp, as shown in fig.2, typically has higher frequency capability and consumes less power than other topologies. Its high-frequency response stems from the fact that its second pole corresponding to the source of the n-channel cascode devices is determined by the transconductance of n-channel devices as opposed to p-channel devices, as in the case of a folded cascode. Also the parasitic capacitance at this node arises from only two transistors instead of three, as in the latter. The single stage architecture naturally suggests low power consumption.

TWO STAGE TELESCOPIC FULLY DIFFERENTIAL OP-AMP

The first step of any two stage design is the design of input differential stage amplifier, which is telescopic differential amplifier in our case. The input transistors of the telescopic cascode stage are NMOS devices to maximize g_m/I_d[7]For the second/output stage, a common source amplifier for each differential output was utilized as typically done. Differential amplifiers as output stage would be more complicated due to the design of another common mode feedback circuit. In addition, the tail current transistor for the differential amp will only consume voltage headroom, thus lowering the output swing. To ensure stability of the amplifiers, miller compensation is used despite the cascode compensation's better high frequency performance. Miller compensation however, can be easily designed and will introduce non-negligible noise depending on how the circuit is compensated.

The two stage topologies may prove inevitable if the output swing voltage swing must bemaximized. Thus, the stability and compensation of such op-amps is of interest. Thecircuit shown in fig.3, we identify three poles: pole at X (or Y), another at E (or F) and third at A (or B). From our foregoing discussion, we know that the pole at X lies at relatively high frequencies.The small signal resistance seen at E in fig.3 is quite high, even the capacitance of M3, M5 and M9 create a pole relatively close to the origin. At node A, the small signal resistance is lower but the value of C_L may be quite high. Consequently, we say that the circuit exhibit two dominant poles. One of the dominant poles must move toward the origin so as to place the gain crossover well below the phase crossover. However, the unity gain bandwidth after compensation cannot exceed the frequency of the second pole of the open loop system. Thus, if the magnitude of $\omega_{P,E}$ is to reduced, the available bandwidth is limited to approximately $\omega_{P,A}$,, a low value. Furthermore, the very small magnitude of the required dominant pole translates to a very large compensation capacitor.The circuit as shown in fig.4 with Miller capacitances gives two poles as follows [6]:

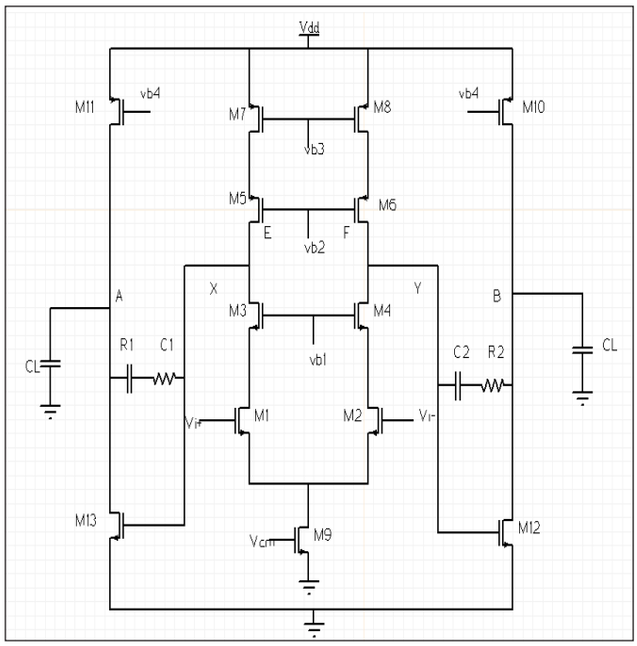


Fig. 3 Two Stage Telescopic Op-Amp

$$W_{p1} \approx \frac{1}{R_s\left[(1+g_{m9}R_L)(C_C+C_{GD9})+C_E\right]+R_L(C_C+C_{GD9}+C_L)} \quad (2)$$

$$W_{p2} \approx \frac{R_S\left[(1+g_{md}R_L)(C_C+C_{GD9})+C_E\right]+R_L(C_C+C_{GD9}+C_L)}{R_S R_L\left[(C_C+C_{GD9})C_E+(C_C+C_{GD9})C_L+C_E C_L\right]} \quad (3)$$

Where, R_S denotes output resistance of the first stage and

$$R_L = r_{o10} \parallel r_{o12} \quad (4)$$

These expressions are based on the assumption $|\omega_{P1}| \ll |\omega_{P2}|$ before compensation, ω_{P1} and ω_{P2} are of the same order of magnitude. For large C_L the magnitude of output pole approximated as

$$\omega_{P2} \approx \frac{1}{(R_L C_L)} \quad (5)$$

and after compensation,

$$\omega_{P2} \approx \frac{g_{m9}}{(C_E+C_L)} \quad (6)$$

In cascode topologies, the zeros are quite far from the origin, in two stage op-amps incorporating Miller compensation, a nearby zero appears in the circuit. The right half plane zero at

$$\omega_Z \approx \frac{g_{m9}}{(C_C+C_{GD9})} \quad (7)$$

This is because $C_C + C_{GD9}$ forms a 'parasitic' signal path from input to output. The presence of right half zero degrades the stability considerably. The right half plane zero in two-stage CMOS op amps, is a serious issue because gm is relatively small and CC is chosen large enough to position the dominant pole properly.

For moving or eliminating zero, there are many method have been develop, one approach is to place a resistor in series with compensation capacitor [6]. thereby modifying the zero frequency. The zero frequency is given by:

$$\omega_Z \approx \frac{g_m}{C_C\left(g_{m9}^{-1}-R_Z\right)} \quad (8)$$

In practice we may even move the zero well into the left half plane so as to cancel the first non-dominant pole. This occurs if

$$\frac{g_m}{C_C\left(g_{m9}^{-1}-R_Z\right)} = \frac{-g_{m9}}{C_L+C_E} \quad (9)$$

that is,

$$R_Z = \frac{C_L+C_C+C_E}{g_{m9}C_C} \quad (10)$$

$$R_Z = \frac{C_L+C_C}{g_{m9}C_C} \quad (11)$$

Because, CE is typically much less than C_L+C_C. The above followed compensation technique is known as nulling resistor compensation technique. The zero position is pushed away with a resistance in series with *Cc*.

$$\frac{V_o}{V_{in}} \approx A_o \frac{1+s\left(R_Z-\frac{1}{g_{m2}}\right)C_C}{\left(1+\frac{s}{P1}\right)\left(1+\frac{s}{P2}\right)} \quad (12)$$

COMMON MODE FEEDBACK CIRCUIT

Fig.4 shows the CMFB circuit using only transistor here. M1 – M4 are matched and always operate in active region. M1 – M2 and M3 - M4 are source coupled pair,that sense the common mode voltage generate the outputwhich is proportional to the difference between V_{oc} and V_{CM}.

The difference input at M1 – M_2 and M3 – M4 are V_{o1} – V_{CM} and V_{o2} – V_{CM} simultaneously. That enough to allow the use of small signal analysis. Assume that the common mode gain of these source coupled pair is zero.

The drain current in M2 and M3 are -

$$I_{d2} = -\frac{I_o}{2} - g_{m2}\left(\frac{V_{o2}-V_{CM}}{2}\right) \quad (13)$$

$$I_{d3} = -\frac{I_o}{2} - g_{m3}\left(\frac{V_{o1}-V_{CM}}{2}\right) \quad (14)$$

The current I_5 is mirrored by tail transistor of the Op-amp.

$$I_{D5} = |I_{D2}| + |I_{D3}| \quad (15)$$

$$= \frac{I_o}{2} + \frac{I_o}{2} \quad (16)$$

$$I_{D5} = I_o \quad (17)$$

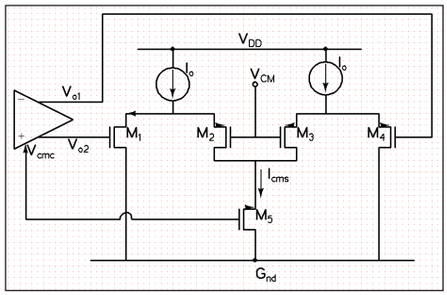


Fig. 4 Common Mode Feedback Circuit

Means we can design to take current through M_5 and Io should be equal or take the W/L of the M_5 same as the W/L of the tail transistor of first stage of fully differential Op-amp.

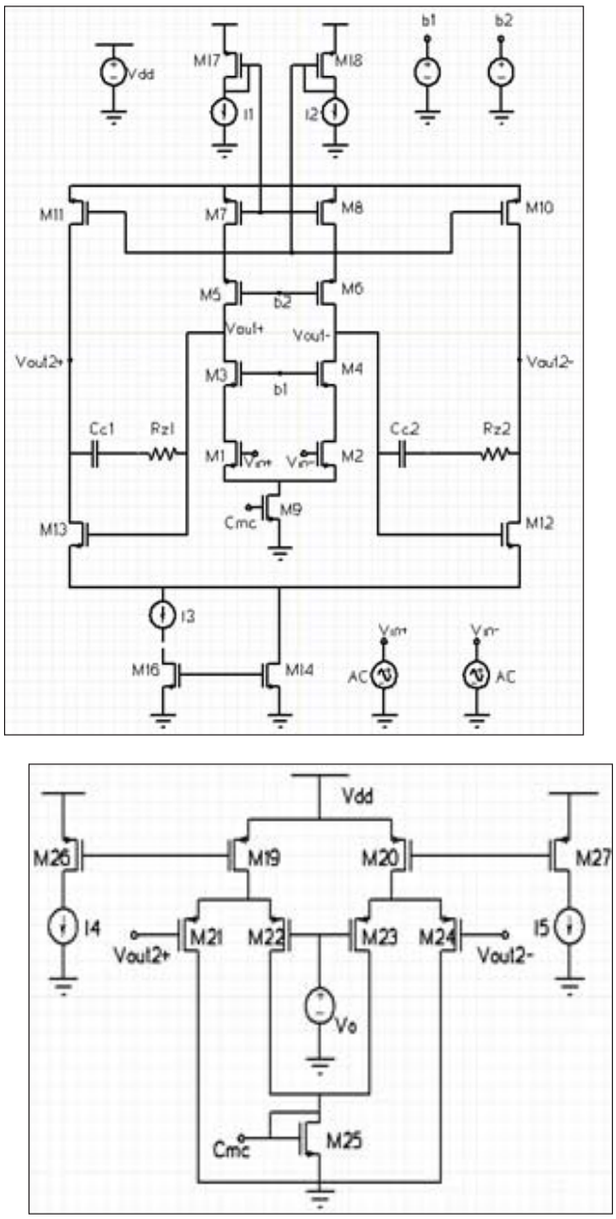


Fig. 5 Two Stage Fully Differential Telescopic Op-amp with CMFB

DESIGN OF OUTPUT STAGE

To design an analog circuit, basic requirement high gain high swing. In two stages Op-amp 1st stage gives the high gain but swing is not enough in first stage. So that second stage is added which provided the highest swing for the Op-amp. Output has sufficient transconductance relative to the load capacitance to meet bandwidth requirements. In our design we use the common source amplifier as a output stage. A common source stage having gate as a input, drain as a output and source is grounded. Common source amplifiers may be viewed as a transconductance amplifiers or as a voltage amplifier. Gain of output stage is given by

$$Av_2 = gm_1 (ro_1 \| ro_2) \quad (18)$$

SCHEMATIC OF PROPOSED FULLY DIFFERENTIAL TELESCOPIC OP-AMP WITH CMFB

The complete schematic of the fully differential telescopic operational amplifier which meets the target specification as table 2. Aspect ratio for all the transistor are given in table 1. All transistor should be in saturation region in fig.5.

Table 1: Aspect Ratio of Transistors and their Functions in Op-amp

TRANSISTOR	**ASPECT RATIO (µ/µ)**
M1 & M2	112.5/0.75
M3 & M4	112.5/0.75
M5 & M6	56.25/0.75
M7 & M8	56.25/0.75
M9	75/0.75
M10 & M11	300/0.25
M12 & M13	300/0.25
M14	900/0.75
M15	705/0.75
M16	12/0.75
M17	11.25/0.75
M18	10/0.25
M19 & M20	120/0.75
M21 ,M22 ,M23,M24	45/0.75
M25	75/0.75
M26	36/0.75

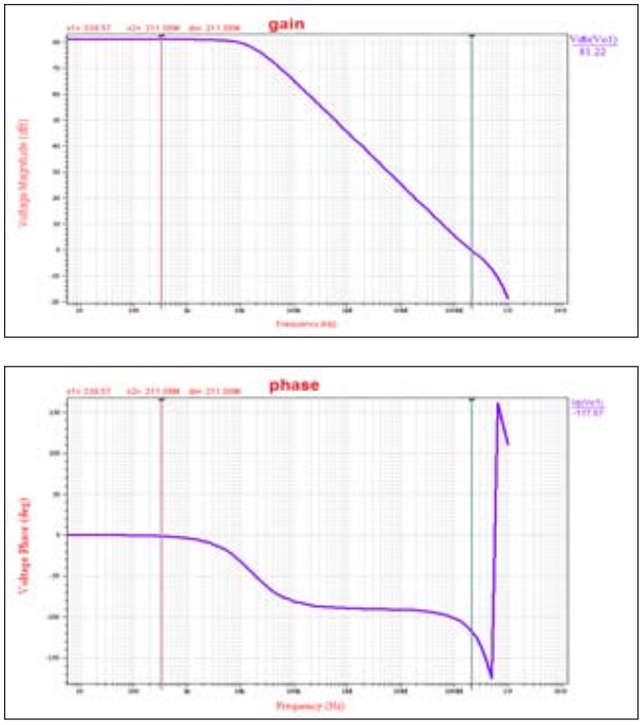


Fig. 6 Frequency Response Plot of Op-amp with with C_L = 4pF

SIMULATION RESULT

The amplifier is powered by supply voltage of 1.8V. The fully differential CMOS Op-amp has been designed and simulated on T-spice 0.25 µm technology. The following section show the simulation result of the final circuit.

AC Analysis-We determined the values of different AC parameter with 1Hz starting frequency and 1GHz stop frequency. We take the output capacitance 4pF. Fig. 6 shows the AC Analysis of Telescopic Op-amp here AC parameters are-

DC gain = 81.22dB

UGB = 211.08MHz

3dB frequency = 12.96 KHz

Common Mode Rejection Ratio-From fig.7differential mode gain is 79.27dB and common mode gain is -11.59, therefore CMRR is 79.27dB – (-11.59) dB = 90.86dB. By using CMFB we increased the CMRR.

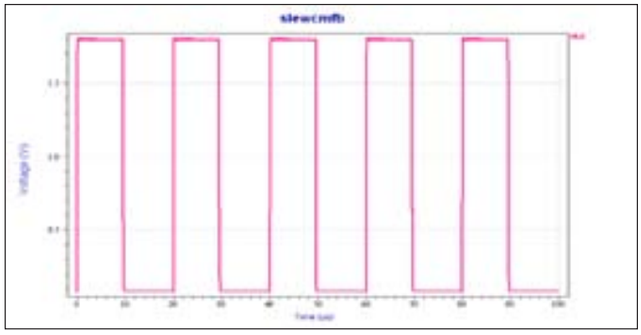


Fig. 7 CMRR of Op-amp with C_L=4pF

Power Supply Rejection Ratio–

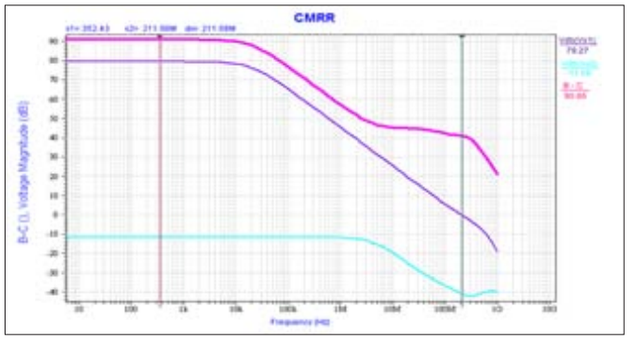


Fig. 8 PSRR of Op-amp with C_L=4pF

From fig.8 gain with AC output is 79.27 dB and gain with AC V_{dd} is 11.90 dB therefore PSRR is 79.27dB–11.90dB = 67.36dB.

Transient Response-Fig. 9 shows the input and output voltage swing, here total output swing is 1.44V (peak to peak).

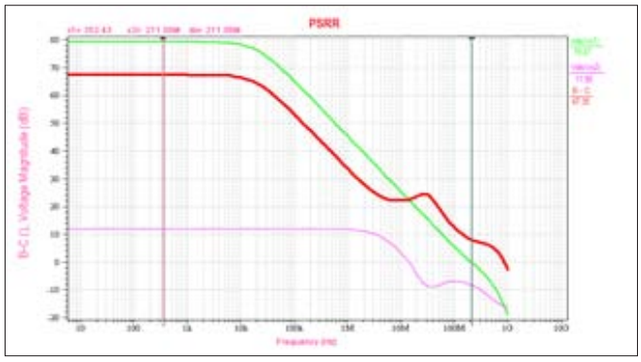


Fig. 9 Transient Response of Op-amp with C_L=4pF

Transient Step Response-

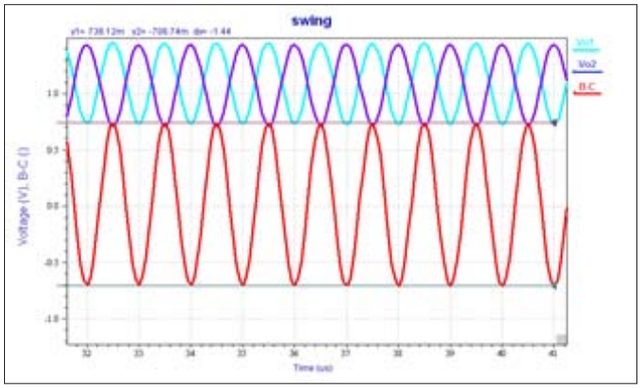


Fig.10 Transient Response of Op-amp with CL

Fig.10 show the transient response of op-amp when load capacitor is 4pF. According to fig.12 transient parameter are-

Slew rate at rising edge = 20.390 V/µs

Slew rate at falling edge = 54.285 V/µs

Settling time = 135.22ns.

CONCLUSION

Operational Amplifier is a very important building block in modern Analog systems. This thesis analyzed the design of two stage fully differential telescopic op-amp with and without common mode feedback. Through simulation, we demonstrated great results from both designs. Telescopic op-amp without CMFB has large gain but small CMRR whereas by using CMFB we can increase CMRR but having less gain as compare without CMFB. The designs were simulated in a 0.25µm CMOS technology. A review of the measured performance of the two designs is shown in Table 3.

The choice of which structure to use would mainly depend on the application. In general, if gain and power dissipation is a main concern then Telescopic Op-amp without CMFB would be the more favorable choice In terms of stability, PM, CMRR and output swing Telescopic Op-amp with CMFB would be a best choice. Overall, both the design are great for analog circuit design application.

Table 3: Performance Summary of Oscillators

Specification	*Target value*	**Simulation result**
Power Supply	1.8V	1.8V
Load capacitance	4pF	4pF
DC open loop gain	≥75dB	81.22dB
Gain bandwidth product	≥200MHz	211.08MHz
Phase margin	≥50^o	62.31^o
3dB frequency	≥5KHz	12.96KHz
CMRR	≥60dB	90.86dB
Output voltage swing	≥1.2V(peak to peak)	1.44(peak to peak)
Slew rate	-	20.39V/µs(rising) 54.28V/µs(falling)
PSRR	-	67.36dB
Setting time	-	135.22ns
Power dissipation	≤10mW	7.50mW

REFERENCES

Yadav, A. (2012). Design of two-stage cmos op-amp and analyze the effect of scaling. *International Journal of Engineering Research and Applications (IJERA)*, 2(5), 647-654.

Grag, P. J. H. P. R., Lewis, S. H., & Meyer, R. G. (2001). *Analysis and design of analog integrated circuits*", (4th Ed.).

Razavi, B. (2002). Design of Analog CMOS Integrated Circuits. McGraw Hill,

Xiyao Z. Design of a High Speed CMOS Fully Differential Op-amp. Retrieved fcrom http://lsm.epfl.ch/files/content/sites/lsm/files/shared/Reports/Bibet_MasterThesis_2008.pdf

Ghavanloo, M. (2004). ECE 703 Class Notes.

Kumar, M. (2009). *Design of Fully Differential Operational Amplifier with HighGain, Large Bandwidth and Large Dynamic Range.* Retrieved from http://dspace.thapar.edu:8080/dspace/bit-stream/10266/923/3/923.pdf

Valle, R. E., & El-Masry, "A Very High-Frequency CMOS Complementary Folded Cascode Amplifier. *IEEE Journals of Solid State Circuits* (vol. 29, No. 2).

Nakamura, K., & Richard Carley, L. (1992). An Enhanced Fully Differential Folded-Cascode OP Amp. *IEEE Journals of Solid State Circuits,* (vol. 27, No. 4, pp 563-568).

Johns, D. A., & Martin K. (1997). *Analog Integrated Circuit Design* (1st Ed.). Textbook, John Wiley & Sons.

Johns, D. A., & Martin, K. (1997). *Analog Integrated Circuit Design* (1st Ed.). Textbook, John Wiley & Sons, First Edition, 1997.

Fully Differential Op-amp (2002). Made Easy by Texas Instruments Apllication Report, SLOA099.

Mortazavi, A. R., & Hassanzadeh, M. R. (2001). *Design Procedure for a High C-Gain and High-Bandwidth Amplifier.* Master of Science Thesis, University of Tehran, Iran.