Design of Ultra Low Power 8 Bit Arithmetic and Logic Unit Using Subthreshold Source Coupled Logic

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Abstract – Designing ultralow power circuits with improved speed and power optimization is a challenging job in the design of a microprocessor. The main component of any processor is the ALU design. STSCL works at very low voltages, consumes less power and has promising performance. In this paper, an ultralow power ALU using STSCL technique in 45nm technology at 1V power supply using cadence virtuoso tools is presented.

Keywords: STSCL, ALU, MCML

I. Introduction

The most serious concerns in the design of integrated circuits today are the design flexibility, power consumption and cost. When there is a restricted source of energy or power, power dissipation and energy consumption become essential point to consider. This leads to the development of many system on chip (SOC) designs through the developments of laptops, cellular phones and many portable systems.

In the design of mixed signal circuits, Subthreshold Source Coupled Logic (STSCL) circuits are notably fascinating where the power dissipation does not depend on the supply voltage [1]. This STSCL circuits operates in the subthreshold region and its speed of operation does not depend on supply voltage and threshold voltage which slackens the design tradeoffs in ultralow power applications.

The power consumption of each STSCL cell can be reduced to few Pico amperes thereby reducing power consumption and it is less sensitive to process and temperature variation's when compared to CMOS technology [2]. STSCL gates are designed which have less logic depth, large activity rate, low output voltage swing and improved power delay product than their CMOS devices.

In this paper a new method of designing digital circuits like arithmetic logic unit for ultralow power applications using STSCL logic is presented.

II. STSCL Logic Families

This logic is constructed using NMOS differential pairs where the operation takes place in the current domain. As all the input and output voltages and currents are differential by nature , this logic has less switching noise [3].

STSCL logic works in subthreshold operation, so important power savings is accomplished for circuits working at low to medium frequencies. Source coupled logic (SCL) or MOS current mode logic (MCML) consists of a group of logic families which mainly consist of three parts, the pull up part consisting of load resistors, the pull down part consisting of NMOS differential pairs and the constant current source Iss (tail bias current) which is obtained from a NMOS transistor. The STSCL inverter circuit which is the basic circuit in this logic consisting of all the above 3 parts is shown below in fig. 1.

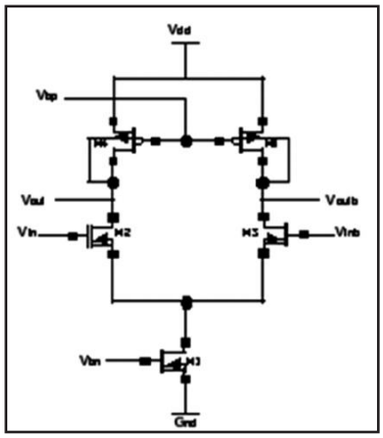

Fig. 1. Circuit of STSCL based inverter/buffer

The logic operation takes place by directing the tail bias current to one of the two load devices which is obtained by the differential NMOS pairs regulated by the differential gate input voltages Vin and Vinb. The output signal is obtained by the two resistors which convert the difference in current in the two branches into differential output voltage Vout and Voutb

In STSCL logic, the load resistors are replaced by PMOS transistors whose bulk and drain are connected to provide a very high resistance so that a very low tail bias current is obtained in the range of few Pico Amperes hence very low power dissipation and less delay are obtained in the designs as given by the equations below [4].

$$\text{Power Dissipation} = V_{DD} \times I_{SS}$$

Thus the output voltage swing V_{swing} of STSCL is decided by the tail bias current I_{SS} and the resistive load R_L.

$$V_{swing} = R_L \times I_{SS}$$

The Time delay is given by

$$\tau_{SCL} = R_L \times C_L = V_{SW} / I_{SS} \times C_L$$

The other STSCL logic gates like NAND/AND, OR/NOR, XOR/XNOR and DFF are shown in the figure 2. These are designed with the help of Binary Decision Diagrams. In the binary decision diagrams, every node specifies a differential pair and every branch show the connection between the drain and the source of an output [5]. The nodes 0 and 1 represent both the complementary outputs of the STSCL gates. An example of two input AND gate, its truth table and the corresponding Binary decision diagram is given in figures 3 and 4

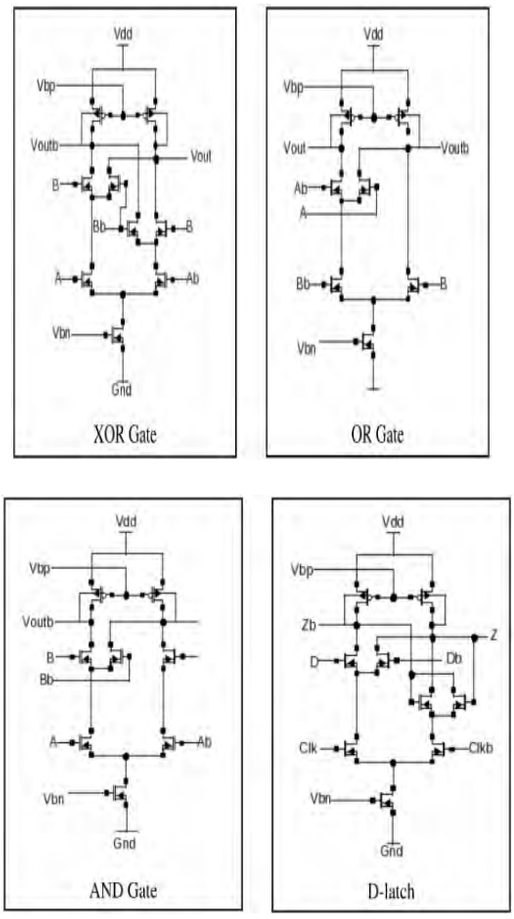

Fig. 2. Different STSCL gates

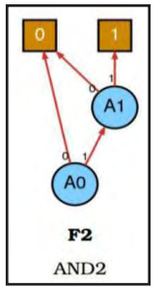

Fig. 3. Binary decision diagram of TWO input AND gate

A	B	out
0	0	0
0	1	0
1	0	0
1	1	1

Fig. 4. Truth Table of two input AND gate

III. STSCL Based ALU

This paper features techniques used for designing an ultra low power Arithmetic and Logic Unit (ALU) using Sub threshold source coupled logic [9]. ALU is the basic component for a simple microprocessor and the central processing unit of a computer. Modern CPUs and Graphics processing units (GPUs) use very powerful and complex ALUs based on the consumers requirement like speed, power and area occupied taken into consideration.

Designing an ALU plays an important role in the ultra low power applications because if the ALUs speed is increased, the whole system performance is improved. Thus designers have to take into consideration constraints like high speed, small area and low power dissipation. The power dissipation, timing, area of an ALU depends on its architecture. So in the place of designing an 8 bit ALU as a one complete circuit it is proposed to design first 1 bit ALU ,then design 2 bit, 4 bit and then finally 8 bit ALU.

1 Bit ALU consists of 8:1 MUX, logic gates, Adder and Sub tractor Circuits. With this design the complexity of the overall circuit reduces and it improves the performance of the circuit The basic operations performed by the ALU are logical operations like AND, OR, NOT and XOR while the arithmetic operations performed are addition, subtraction , increment and decrement [10]. Based on the selection lines of the multiplexer the required arithmetic and logical operations are obtained at the output of the ALU as shown in the truth table below in table 1.

TABLE I
OPERATION OF 1 BIT ALU

S2	*S1*	*S0*	*Operation*
0	0	0	Decrement
0	0	1	Addition
0	1	0	Sub traction
0	1	1	Increment
1	0	0	AND
1	0	1	XOR
1	1	0	NOT
1	1	1	OR

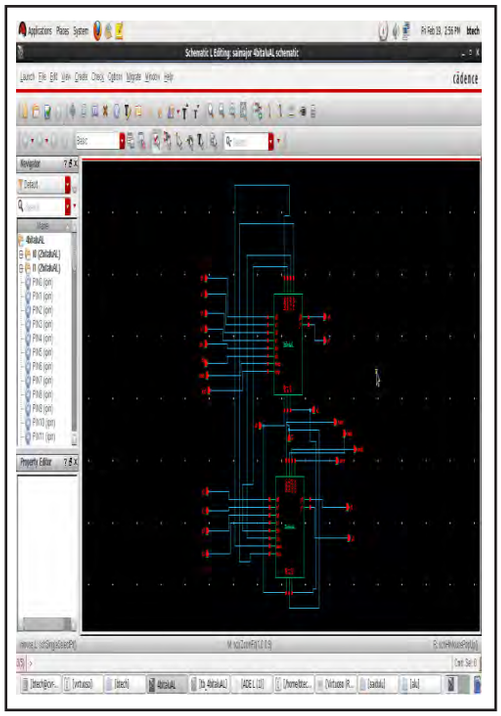

Fig. 5. Schematic of 4 Bit ALU

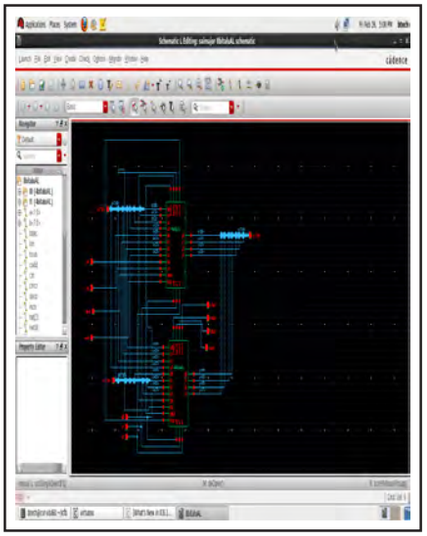

Fig. 6. Schematic of 8 Bit ALU

In 1 bit ALU design, the increment and the decrement operation is obtained by adding or subtracting bit "1" to the input in the STSCL based half adder and half sub tractor circuits [7]. Addition and subtraction is achieved with the help of STSCL based full adder and full sub tractor circuits with carry in/ borrow in given. The logic operations are performed with the help of STSCL based AND, OR and XOR gates. Fig. 5 and 6 show the schematics of 4 bit ALU and 8 Bit ALU.

IV. SIMULATION RESULTS

The simulation results of 8 bit ALU using STSCL Logic in 45nm CMOS technology using Cadence virtuoso tools for a power supply of 1V with a power dissipation of 1.876 m W are presented [11]. The inputs and outputs of 8 bit ALU are shown from fig 7 to fig. 9.

Fig. 7. Inputs a[0] to a[7] and b[7] to b[4] of 8 Bit ALU

Fig. 8. Inputs b[0] to b[7] of 8 Bit ALU

Fig. 9 Outputs y [0] to y[7] of 8 bit ALU

The Power and Delay calculations of STSCL logic gates in 180nm and 45nm technology [7] is shown in the below table 2.

TABLE 2
POWER AND DELAY OF BASIC GATES

Basic Gates	*Power and delay in 180nm*		*Power and Delay in 45nm*	
	Power(W)	*Delay(sec)*	*Power(W)*	*Delay(sec)*
Inverter	3.12E-3	15.16E-9	7.28E-6	25.32E-12
OR	2.51E-3	45.6E-9	18.76E-6	19.88E-12
AND	9.07E-3	87.1E-9	22.96E-6	10.04E-12
XOR	8.46E-3	67.88E-9	9.17E-6	20.28E-12
NOR	4.31E-3	75.1E-9	18.76E-6	10.1E-9
NAND	6.62E-3	44.87E-9	22.9E-6	28.33E-12
XNOR	3.16E-3	60.2E-9	9.17E-6	15.24E-9

V. CONCLUSION

In this paper the strength of STSCL circuits as an alternative solution for implementing ultra low power digital systems is explored. STSCL topology is growing as an significant research area in the recent years due to its lower power dissipation which is mainly necessary in low power digital circuits In this paper a new architecture of 8 bit ALU using STSCL technique is presented. Every block of ALU is designed using STSCL gates. By doing this considerable power reduction and good performance is achieved [6].

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