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Design and Optimization of FINFET Digital Circuits

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Abstract – Over the last two decades, low-power design has become a concern in digital VLSI design, especially for portable and high performance systems. Large scale integration (LSI) has become so dense that a single silicon LSI chip may contain tens of thousands of transistors. Scaling of technology node increases power-density more than expected. CMOS technology beyond 65nm node represents a real challenge for any sort of voltage and frequency scaling Starting from 120nm node, each new process has inherently higher leakage current density with minimal improvement in speed. Low cost always continues to drive higher levels of integration, whereas low cost technological breakthroughs to keep power under control are getting very scarce. It is therefore necessary to look at other more revolutionary options like change in transistor structure from the traditional planar transistors. FINFET technology has been born as a result of increase in the levels of integration. Simulation is done in tanner tool in 45nm technology. Comparisions between CMOS and FINFET is clearly shown.

Keywords: CMOS, DGMOSFET, FINFET, Ion/Ioff, Low Power, Power Dissipation, Leakage Current

I . Introduction

During the desktop PC design era VLSI design efforts have focused primarily on optimizing speed to realize computation intensive real-time functions such as video compression, gaming, graphics etc [9]. As a result, we have semiconductor ICs that successfully integrated various complex signal processing modules and graphical processing units to meet our computation and entertainment demands. The strict limitation on power dissipation in portable electronics applications such as smart phones and tablet computers must be met by the VLSI chip designer while still meeting the computational requirements.

While wireless devices are rapidly making their way to the consumer electronics market, a key design constrain for portable operation namely the total power consumption of the device must be addressed. Reducing the total power consumption in such systems is important since it is desirable to maximize the run time with minimum requirements on size, battery life and weight allocated to batteries [2], [5]. So the most important factor to consider while designing SoC for portable devices is 'low power design [1], [7]. Static power and Dynamic power dissipation grows rapidly. Overall power is dramatically increasing. If the semiconductor integration continues to follow Moore's Law, the power density inside the chips will reach far higher than the rocket nozzle [7]. Power dissipation is the main constrain when it comes to Portability.

II. Finfets

A. FinFet Background

1) FinFet technology has been born as a result of relentless increase in the levels of integration.
2) To achieve the large levels of integration many parameters have changed. Fundamentally the feature sizes have reduced to enable more devices to be fabricated within a given area [5].
3) However other figures such as power dissipation and line voltage have reduced along with increased frequency performance.
4) There are limits to the scalability of individual devices and as process technologies shrink towards 50nm,it became impossible to achieve proper scaling of various device parameters [2].
5) It is therefore necessary to look at other more revolutionary options like change in transistor structure from the traditional planar transistors [1].

These effects make it harder for the voltage on a gate electrode to deplete the channel underneath and stop the flow of carriers through the channel – in other words, to turn the transistor Off.

Comparision:

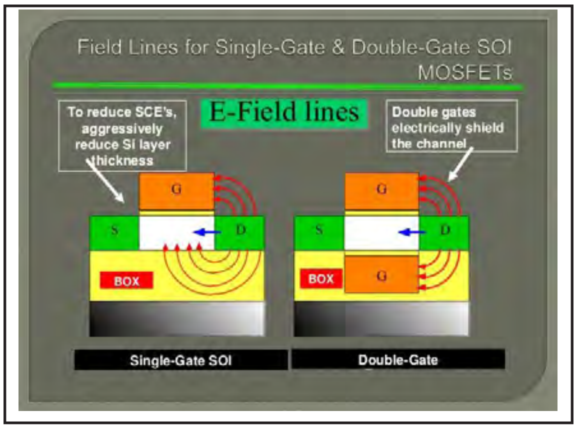

Fig. 1. CMOS and DG MOSFET

B. Advantages of FinFet technology

Power: Much lower power consumption allows high integrational levels. Early adopters reported 150% improvements.

Operating voltage: FinFets operate at a lower voltage as a result of their Threshold voltage.

Feature size: Possible to pass through the 20nm barrier previously thought as an end point [5].

Static leakagecurrent:Typically reduced by upto 85% [6]

Operating speed: Often in excess of 30% faster than the non-FinFet versions.

III. Simulation Results

A. NMOS

NMOS circuit is designed in tanner tool at 45nm technology.

L=0.045µm W=0.045µm

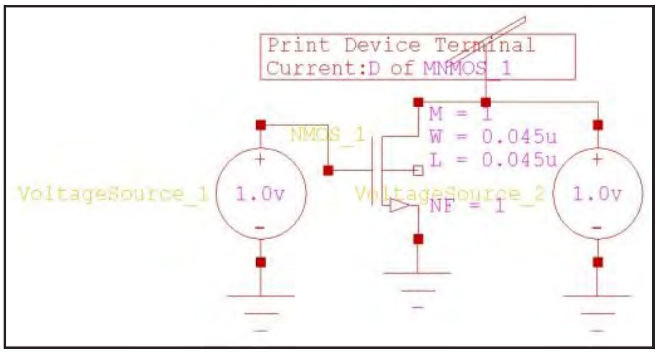

Fig. 2. Circuit diagram of NMOS

Ids wrt Vgs is found at different vds.

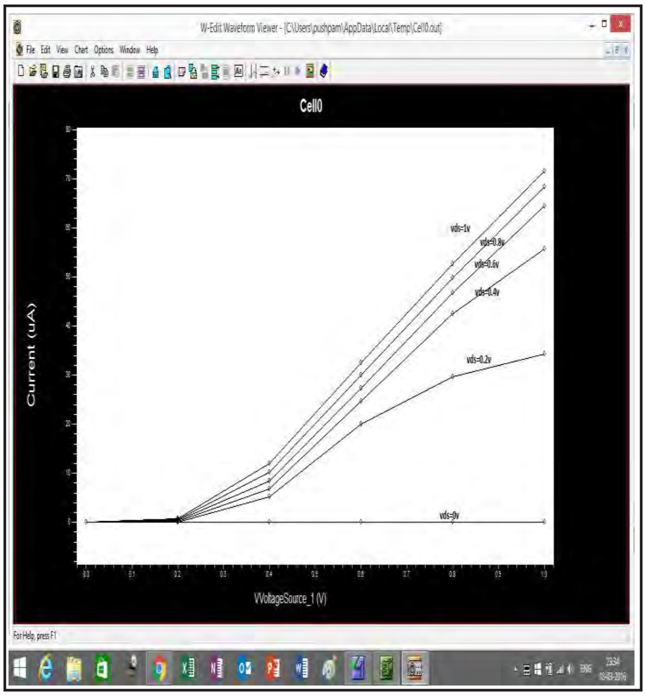

Fig. 3. IV characteristics of NMOS

Table I
Ids vs Vgs WRT Vds=0.2v For NMOS

Vgs	*Ids(NMOS)µ amps*
0v	0.007693
0.2v	1.344
0.4v	52.13
0.6v	200.4
0.8v	296
1v	343.2

B. FinFet NMOS

NMOS FinFet circuit is designed in tanner tool at 45nm technology.

L=0.045µm W=0.045µm

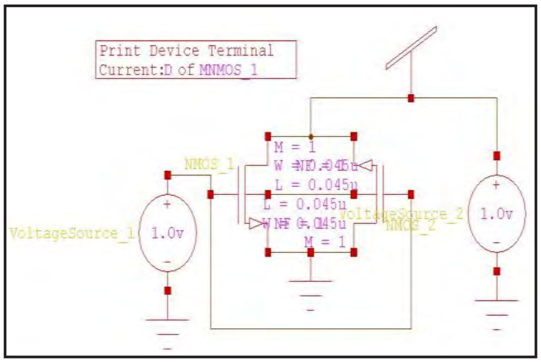

Fig. 4. Circuit diagram of finfet NMOS

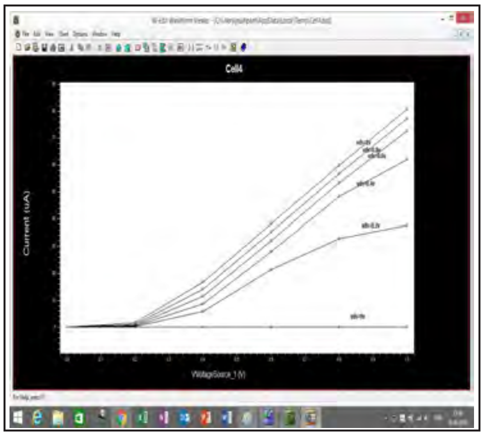

Fig. 5. IV characteristics of Finfet NMOS

TABLE II
IDS VS VGS WRT VDS=0.2V FOR FINFET NMOS

Vgs	*Ids(NMOS FinFet)µ amps*
0v	0.001132
0.2v	0.1789
0.4v	5.98
0.6v	21.35
0.8v	32.8
1v	37.01

Comparisions :

TABLE III
COMPARISION IDS VS VDS FOR BOTH NMOS AND FINFET NMOS

Vgs	*Ids(NMOS)µ amps*	*Ids(NMOS FinFet)µ amps*
0v	0.007693	0.001132
0.2v	1.344	0.1789
0.4v	52.13	5.98
0.6v	200.4	21.35
0.8v	296	32.8
1v	343.2	37.01

Ion/Ioff :

TABLE IV
ION AND IOFF OF NMOS AND NMOS FINFET

Off current On current

Vds	*Ids(NMOS) µamp*	*Ids(Fin) µamp*	*Ids NMOS*	*Ids(Fin) µamp*
0v	0	0	0	0
0.2v	0.0076	0.00113	34.5	38
0.4v	0.0014	0.00030	56.3	62.5
0.6v	0.0027	0.00737	64	73.5
0.8v	0.00512	0.00147	68	78
1v	0.009	0.0026	72	81.5

C. Inverter CMOS

Inverter circuit is designed in tanner tool at 45nm technology.

L=0.045µm W=0.045µm

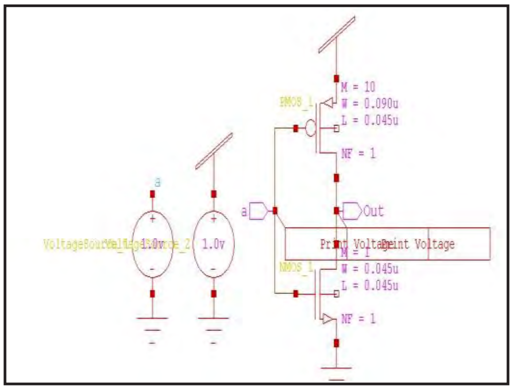

Fig. 6. Circuit inverter CMOS

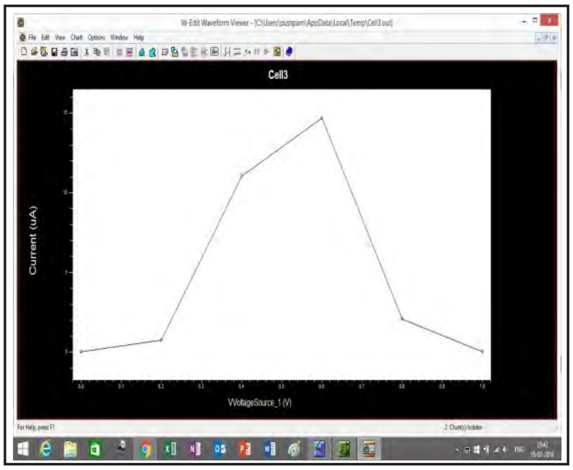

Fig. 7.

IV. CHARACTERISTICS OF INVERTER

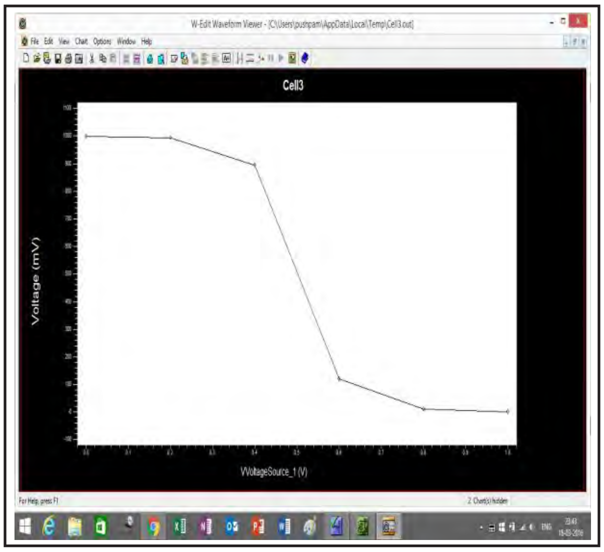

Fig. 8. DC characteristics of inverter

Table V: Vin Vs Vout Is Observed

Vin(volts)	*Vout(inv)milli volts*
0	999.80
0.1	999
0.2	990.
0.3	960.
0.4	900.
0.5	499.8
0.6	120.
0.7	80
0.8	10
0.9	5
1	0.01

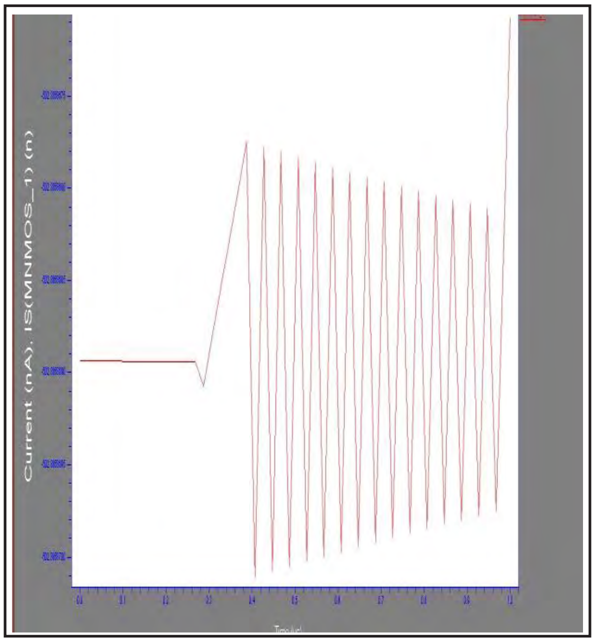

Fig. 9. Leakage current waveform CMOS inverter

Table VI: Leakage Current WRT Time is Observed

Time (μ sec)	*Leakage current(nano amps)*
0	502.88587
0.1	502.88586
0.2	502.88585
0.3	502.88587
0.4	502.88587
0.5	502.88587
0.6	502.88586
0.7	502.88585
0.8	502.88585
0.9	502.88586
1	502.88587

Average leakage current = 502.88nano amps.

FinFet Inverter

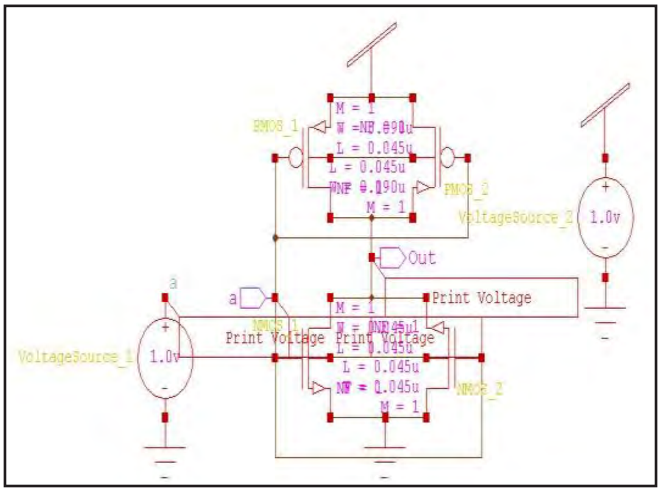

Fig. 10. Circuit diagram of finfet inverter

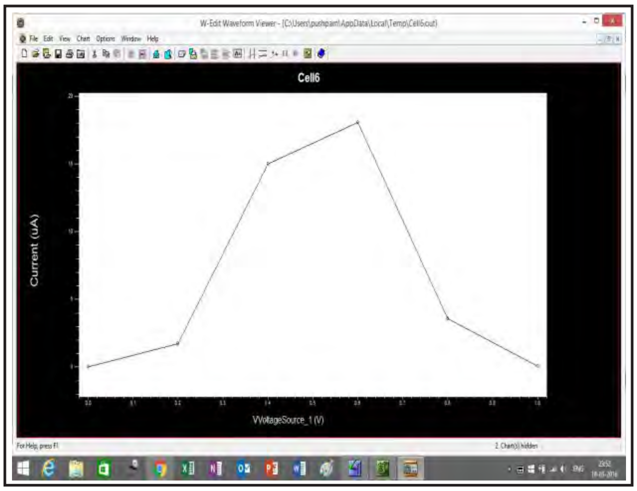

Fig. 11. IV characteristics of finfet inverter

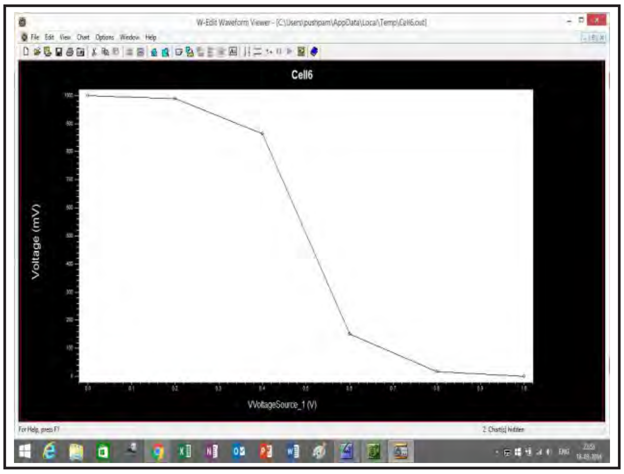

Fig. 12. DC characteristic of finfet inverter

Table VII
Vin vs Vout is Observed

Vin(volts)	*Vout(finfet inv)milli volts*
0	1000
0.1	990
0.2	980
0.3	940
0.4	860
0.5	500
0.6	150
0.7	90
0.8	20
0.9	10
1	0

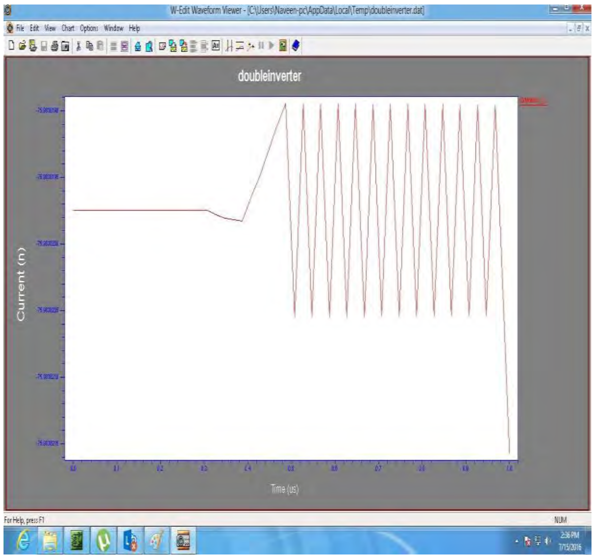

Fig. 13. Leakage current waveform finfet inverter

Table VIII: Leakage Current WRT Time is Observed

Time (μ sec)	*Leakage current(nano amps)*
0	75.9838
0.1	75.9836
0.2	75.9838
0.3	75.9837
0.4	75.9836
0.5	75.9837
0.6	75.9838
0.7	75.9837
0.8	75.9836
0.9	75.9837
1	75.9836

Average leakage current =75.98 nano amps.

Power Consumption:

$$P=V*I$$

From the above simulation we observe that the current

is reduced in Finfet compared to MOSFETs. As I is reduced Power is also reduced. Power consumption of FinFet is reduced.

Power consumption of NMOS: 0.716 μwatts

Power consumption of NMOS FinFet: 0.0016μ watts.

Power consumption of inverter: 0.0334μ watts

Power consumption of FinFet inverter: 0.01160197μ watts

IV. Conclusion

Hence we can say from the above analysis FINFET is better than CMOS technology in terms of power consumption, Ion/Ioff ratio, DC characteristics and leakage currents. Average leakage current in CMOS inverter is 502.8namps while in FINFET is 75.98namps. Approximately 85% improvement is observed.

References

[1] P. Sharma, S. Khandelwal, and S. Akashe, ‘’Design and optimization of Finfet based schmitt trigger,” *IEEE Fifth International Conference on Advanced Computing & Communication Technologies,* 2015.

[2] J. Kao, A. Chandrakasan, and D. Antoniadis, “Transistor Sizing Issues and Tool for Multi Threshold CMOS Technology,” *Design Automation Conference,* pp. 409-414, 1997.

[3] J. Kao, S. Narenda, and A. Chandrakasan, “MTCMOS hierarchical sizing based on mutual exclusive discharge patterns,” *Design Automation Conference,* pp. 495-500, 1998.

[4] M. Takamiya, K. Nose, H. Kawaguchi, T. Hiramoto, and T. Sakurai, “Boosted Gate MOS (BGMOS): Devid circuit cooperation scheme to achieve leakage-fiee giga-scale integration,” *Proc. CICC,* pp. 409-412, May 2000.

[5] T. Ghani et al.,“Scaling challenges and device design requirements for high performance sub-50 nm gate length planar CMOS transistors,” *Proc. Symp. VLSI Tech., Dig. Tech. Papers,* pp. 174-175, June 2000.

[6] A. Islam, and M. Hasan, “Leakage characterization of 10T SRAM Cell,” *IEEE transactions on electron devices,* vol. 59, no. 3, March 2012.

[7] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, “Low-power Digital CMOS Design,” *IEEE Journal of Solid State Circuits,* pp. 473-484, April 1992.

[8] M. Horowitz, T. Indermaur, and R. Gonzalez, “Low-Power Digital Design,” *Proceedings of the Symposium on Low Power Electronics,* 1994.

[9] S. Borkar, “Design Challenges of Technology Scaling,” *IEEE Micro,* p. 23, July/August 1999.