Design of PLL Using CSVCO in 45N m Technology

Dr. D. R. V. A. Sharath Kumar[1], Mr. J. Nageswara Reddy[2], Mr. A. Dileep[3]
[1]Professor, Department of ECE, St. Martins Engineering College, Hyderabad, Telangana, India.
[2, 3]Assistant Professor, Department of ECE, CMR College of Engineering & Technology, Hyderabad, Telangana, India.
Email: professor.smec@gmail.com[1]

Abstract – Phase-Locked Loop, an electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e., lock) on the frequency of an input, or reference signal. A PLL ensures that a communication signal is locked on a specific frequency and can also be used to generate, modulate and demodulate a signal and divide a frequency. PLL is used often in wireless communications where the oscillator is usually at the receiver and the input signal is extracted from the signal received from the remote transmitter. Design a low power fast-locking PLL by reducing delay and power consumption in gpdk 45nm technology using cadence virtuoso environment. For this purpose, we have designed various individual blocks of PLL by taking into consideration various parameters and simulated. The various blocks are Phase Frequency Detector (PFD), Charge Pump, Loop Filter, Current starved Voltage Controlled Oscillator CSVCO) and Frequency Divider (FD). Here current starved voltage controlled oscillator have been considered for superior performance in form of low power consumption and wide tunable frequency range. The simulation is carried out in the Spectra simulator. The simulation results of PLL and its blocks are reported in this work. It is found that the designed PLL consumes 81.63 uW power from a 1.8V D.C. supply and have a lock time41.47ns.

Keywords: PLL, PFD, CS-VCO, Concepts of Lock range, Lock time, Jitter, Dead zone and passive Low pass filters.

I. Introduction

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL is capable of tracking the phase changes that falls in this bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock CKref to produce a high-frequency clock CKout this is known as clock synthesis. A PLL has a negative feedback control system circuit. The main objective of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is achieved after many iterations of comparison of the reference and feedback signals. In this lock mode the phase of the reference and feedback signal is zero. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant [1].

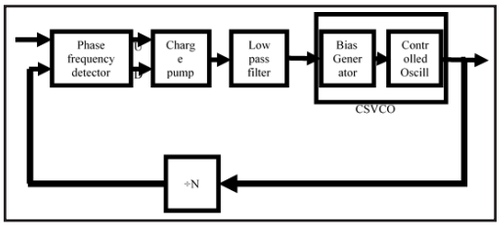

Fig. 1. Block diagram of PLL

II. Proposed Circuit for PLL

The basic operations of a PLL can be divided into three steps. First, the Phase frequency detector (PFD) catches the phase difference between two inputs and generates an error signal Ve whose average value is linearly proportional to the phase difference. A Loop filter (LF) is then used to suppress the high-frequency components of the PFD output, allowing the average value (DC or low-frequency) to control the VCO frequency. Finally, an oscillator generates an output signal whose frequency is a linear function of the control signal out of the LF. The generated signal is fed back to the input of the PFD [2] and another phase comparison is started until the phase difference achieves a fixed relationship. Reference and Output waveforms of a PLL is shown in fig 2.

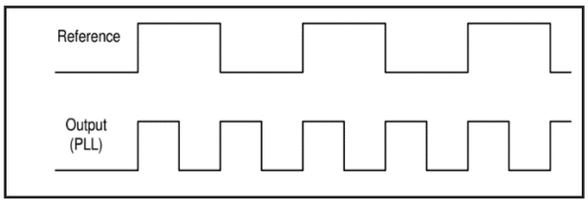

Fig. 2. Reference and Output waveforms of a PLL

III. Schematic Designs

A. Phase Frequency Detector

The Phase frequency Detector (PFD) is one of the main parts in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals UP and DOWN. Figure 3 shows a traditional PFD circuit.

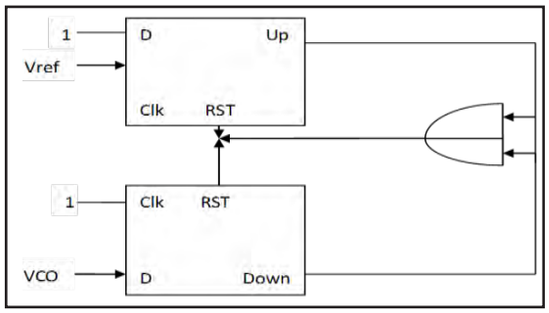

Fig. 3. Block diagram of a traditional PFD circuit

B. Explanation of PFD Block

If there is a phase difference between the two signals, it will generate “UP” or “DOWN” synchronized signals. When the reference clock rising edge leads the feedback input clock rising edge “UP” signal goes high while keeping “DOWN” signal low. On the other hand if the feedback input clock rising edge leads the reference clock rising edge “DOWN” signal goes high and “UP” signal goes low. Fast phase and frequency acquisition PFDs are generally preferred over traditional PFD. The general circuit diagram PFD is shown in the Figure 3.5. As it was described above, it is composed by two D-FF and an AND logic gate. Each DFF has got eight CMOS transistors and the AND gate has got six ones. So, this design consists of 22 transistors. Test bench of PFD is shown in fig 5 [4].

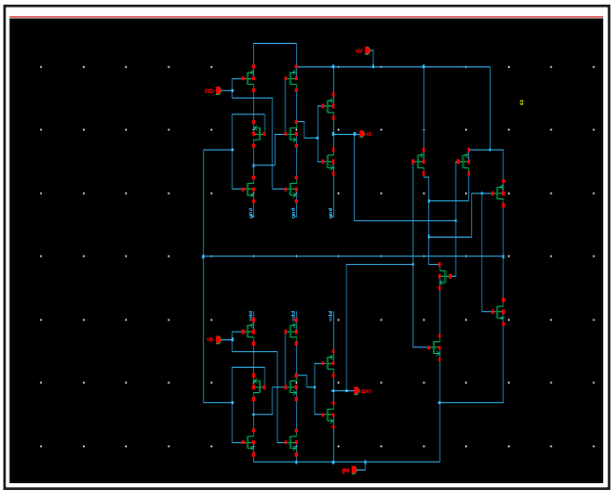

Fig. 4. Schematic diagram of PFD circuit

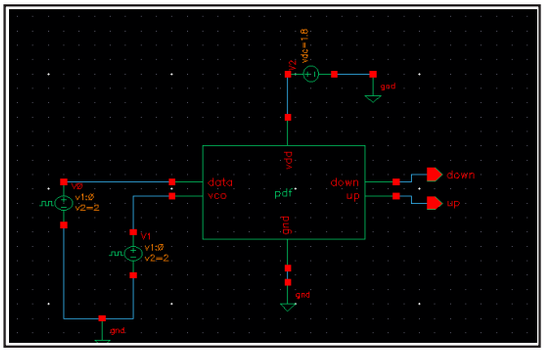

Fig. 5. PFD test bench

C. Charge Pump

A charge pump circuit is used to convert the digital signal from the phase frequency detector to analog signal, the output of which is used to control the frequency of the voltage control oscillator. The output of the PFD should be combined into a single output to drive the loop filter. In below Fig charge pump, two NMOS and two PMOS are connected serially. The uppermost PMOS and lowermost NMOS are considered as the current source and the other PMOS and NMOS in the middle are connected to the “Up” and “Down” of the output of PFD, respectively When the PFD “Up” signal goes high, the PMOS will turn on. This will connect the current source to the loop filter. It is in the similar way when the PFD “Down” signal goes high. The schematic of charge pump is shown in fig 6 and charge pump test bench is shown in fig 7.

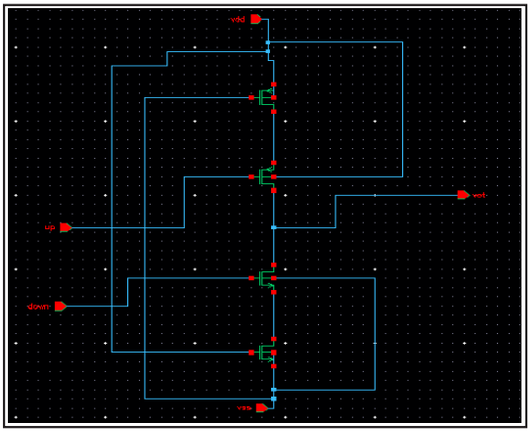

Fig. 6. Schematic diagram of the charge pump

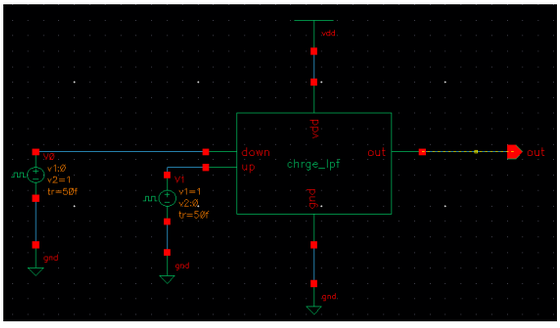

Fig. 7. Charge pump test bench

D. Low pass Filter

Filters are frequently added after the charge pump to reduce the ripple. The function of the loop filter is to convert the output signal of phase frequency detector to control voltage and also to filter out any high frequency noise introduced by the PFD. The loop filter shown in Fig 8. used with this type of PFD is a simple RC low-pass filter.

Since the output of the PFD is oscillating, the output of the loop filter will show a ripple as well, even when the loop is locked. This modulates the clock frequency, an unwanted characteristic of a DPLL using PFD. A ripple on the output of the loop filter with a frequency equal to the clock frequency will modulate the control voltage of the VCO. A high speed low power consumption positive edge triggered Delayed (D) flip flop was designed for increasing the speed of counter in Phase locked loop, using 45nm CMOS technology.

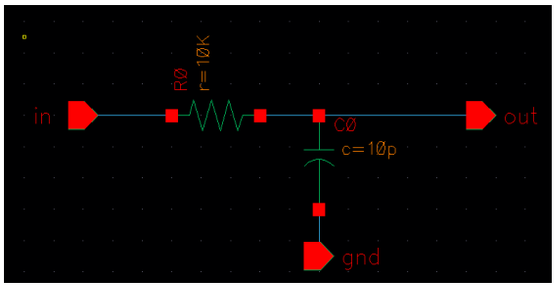

Fig. 8. Schematic of low pass filter

Current starved Voltage Controlled Oscillator

The operation of current starved VCO is similar to the ring oscillator. An oscillator is an autonomous system which generates a periodic output without any input. The most popular type of the VCO circuit is the current starved voltage controlled oscillator (CSVCO). Here the number of inverter stages is fixed with 5. The simplified view of a single stage current starved voltage controlled oscillator is also shown in fig. 9.

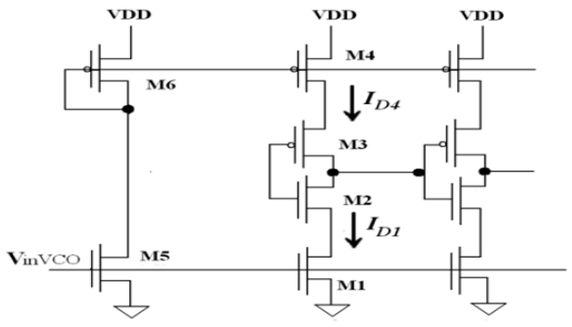

Fig. 9. Simplified view of a single stage current starved VCO

Transistors M2 and M3 operate as an inverter while M1 and M4 operate as current sources. The schematic diagram of CS-VCO is shown in fig 10 and test bench is shown in fig 11.

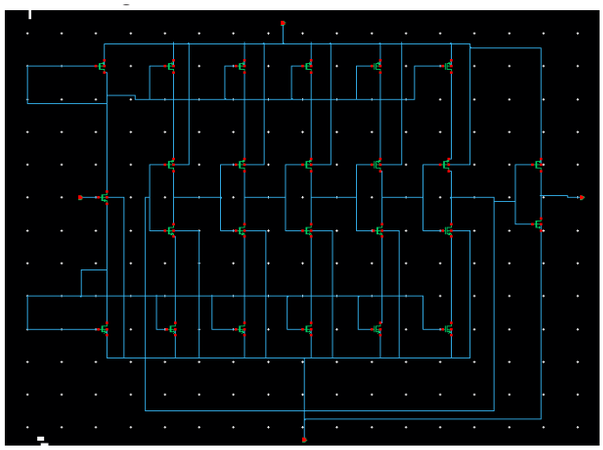

Fig. 10: Schematic diagram of a current starved VCO.

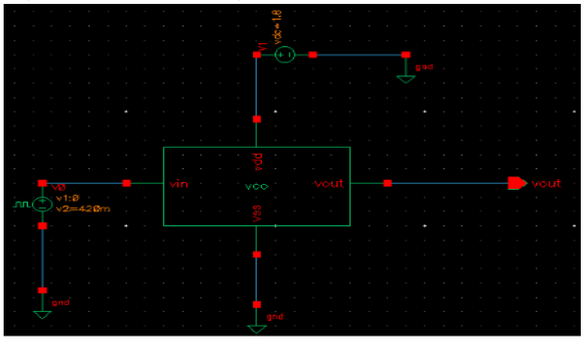

Fig. 11:CS VCO Test bench

E. Frequency Divider

Frequency divider divides the VCO frequency to generate a frequency which is comparable with reference frequency. Here we used divide by 2 network, we can vary the divider network for synthesis of different frequencies. It divide the clock signal of VCO and generate d clock [6] which can be easily compared with that of applied phase frequency The output of the VCO is fed back to the input of PFD through the frequency divider circuit. The frequency divider in the PLL circuit forms a closed loop. It scales down the frequency of the VCO output signal. A simple D flip flop (DFF) acts as a frequency divider circuit. The schematic of a simple DFF based divide by 2 frequency divider circuit is shown in the Fig. 12.

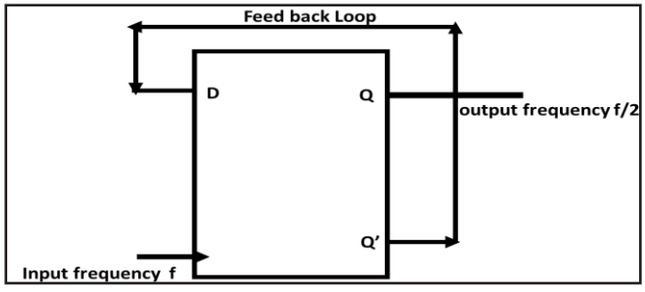

Fig. 12. Simple DFF based divide by 2 frequency divider circuit

The Schematic diagram of divide by 2 frequency divider circuit is shown in the Figure 13 and test bench is shown in fig. 14.

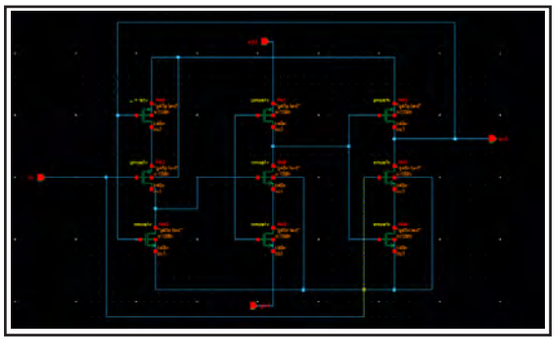

Fig. 13. Schematic diagram of divide by 2 frequency divider

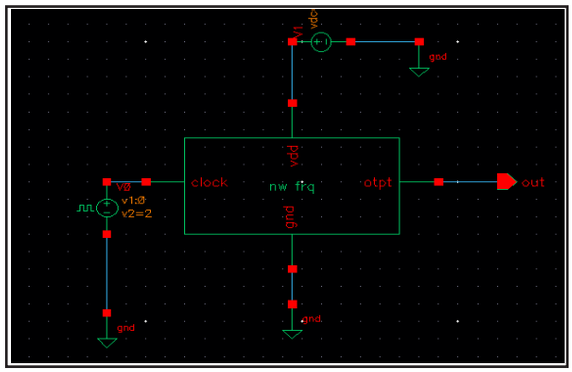

Fig. 14. Divide by 2 frequency divider test bench

F. Terms in PLL

Lock in Range

Once the PLL is in lock state that range of frequencies is called as lock in range. This is also called as tracking range or holding range.

Capture Range

When the PLL is initially not in lock, what frequency range can make PLL lock is called as capture range. This is also known as acquisition range. This is directly proportional to the LPF bandwidth.

Reduction in the band signals, but at the same time phase margin becomes poor. Illustration of lock and capture range is shown in fig. 15.

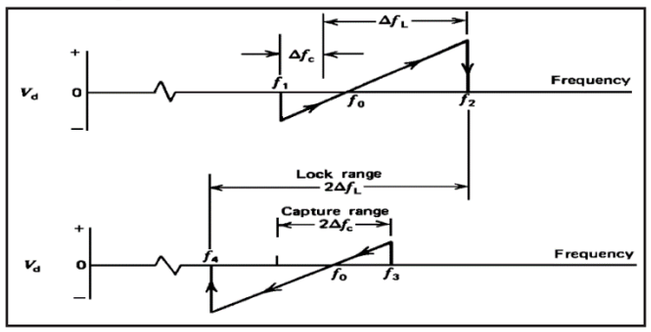

Fig. 15. Illustration of lock and capture range

Pull in Time

The total time taken by the PLL to capture the signal (or to establish the lock) is called as Pull in Time of PLL. It is also called as Acquisition Time of PLL.

IV. Results

After the theorist study of each design, it is necessary to verify the properties of which boast. The parameters that will be analyzed are the ones that describe the operation of this kind of circuits: transient response, the delay time/reset time and the power consumption. For the simulations in CADENCE the used technology is 45nm CMOS technology. Below, the analysis parameters from which the designs will be analyzed are briefly described**:**

A. Transient Response

It is the response of a system to a change from equilibrium. In this case, the input signals, that active the circuit, are some periodic succession of pulses and this causes some variations in the outputs of the circuit. In the following simulations the duration is 20ns**.**

B. Delay Time: These Parameters are Usually the

bottleneck in the PLL designs. These circuits are called to be as faster as possible. So, the delay time and the reset time must be the shorter the better. The delay time is measured as the difference in time between the input signal and the output one (in the half maximum voltage value) that ideally would be zero but it depends on the circuit structure so it is difficult to reduce.

C. *Power consumption:* To measure the power consumption of a circuit, it is necessary to know the voltage value and the average current value in a period. It must be measured in the supply voltage node. According to that, to obtain the average current its wave must be integrated in a period. Afterwards, it must be divided by the period length. Then, P=VI. The power is expensive, so it is interesting to work with low power consumption designs.

D. Results of PFD

As it was described above, it is composed by two D-FF and an AND logic gate. Each D- FF has got eight CMOS transistors and the AND gate has got six ones. So, this design consists of 22 transistors**.**The obtained waveforms of Transient response analysis of Phase frequency detector as shown in below fig 16:

E. Transient response of PFD

Realizing the transient simulation, the obtained waves are illustrated in figure. As it is shown on it, the input signals ‘(F

ref)' and '(F vco)' have different frequency and phase. Besides, the A signal (which is the D-FF output whose input is F ref) follows F ref input until the reset signal is activated. The same happens with B signal (which is the D-FF output whose input is (Fvco) and (Fvco). Moreover, reset signal (which is the AND gate output) is active only when both A and B are up.

It is observable, also, that as it is said in previous chapters, when Fref presents an instantaneous frequency higher that (Fvco), A ("up signal") increases its value, maintaining B ("down signal") zero. Additionally, when both (Fref) and (Fvco) have the same frequency, both A ("up") and B ("down") signals become zero.

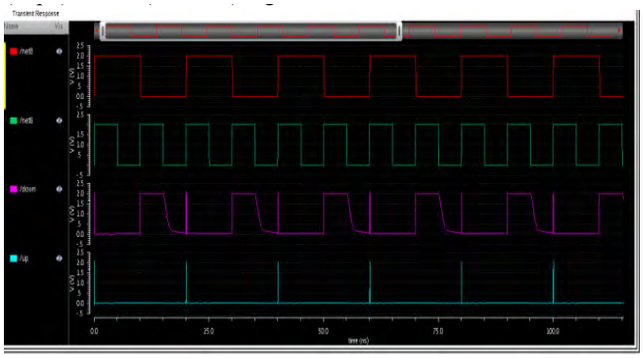

Fig 16: Result of PFD Block

F. Results of Charge Pump

Charge pump is the next block to the phase frequency detector. The output signals - UP signal and DOWN signal generated by the PFD is directly connected to the charge pump. Charge pump converts the phase or frequency difference information into a voltage, used to tune the VCO. Charge pump circuit is used to combine both the outputs of the PFD and give a single output which is fed to the input of the filter. It gives a constant current which should be insensitive to the supply voltage variation. The amplitude of the current always remains same but the polarity changes which depends on the value of the "UP" and "DOWN" signal. The output of the charge pump is connected to a low pass filter that integrates the charge pump output current to an equivalent VCO control voltage (Vcntl). It charges or discharges the current of the charge pump related to the value of the error signal (pulse width of the UP signal or DOWN signal) generated by the PFD. Results of charge pump is shown in fig 17.

G. Transient Response of Charge Pump

When the reference signal clock edge leads the feedback clock edge, the UP signal of the PFDgoes high. So to make both the clock have rising edge at the same time the VCO output signal frequency has to be increased. For this purpose an increase in control voltage is needed from the output of charge pump and loop filter circuit. When the rising of feedback signal leads the reference signal rising edge the control voltage decreases for the period during which the DOWN signal of the PFD remains high.

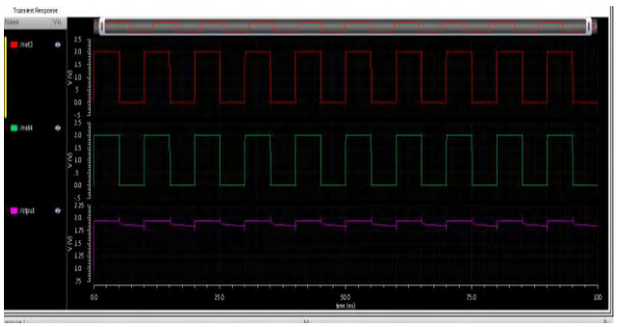

Fig 17: Result of charge pump

H. Results of CS VCO

A voltage controlled oscillator (VCO) is one of the most important basic building blocks in analog and digital circuits. A ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. This current starved VCO is designed using ring oscillator and its operation is also similar to that.

I. Transient response of CS VCO

The simulation of Current Starved VCO is done in Cadence software using 45 nm CMOS technology. There are two number of buffers. The tuning range of the VCO is from 7.5MHz to 832MHz. The center frequency is 200MHz for a control voltage of 0.42V. The below figure 18 shows the transient response of VCO. The gain of the VCO is 500MHz/V.

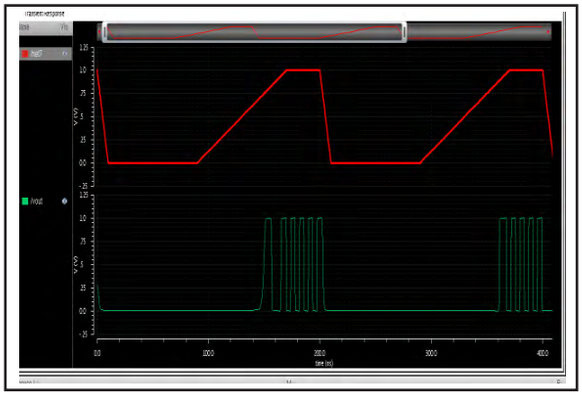

Fig 18: Transient response of CS VCO

J. Results of Frequency Divider

The output of the CS VCO is fed back to the input of PFD through the frequency divider circuit. The frequency divider in the PLL circuit forms a closed loop. It scales down the frequency of the CS VCO output signal.

K. Transient Response of Frequency Divider

The transient response of the frequency divider is shown in the fig. 19. Here, the VCO output frequency is 100MHz and is divided by 2 which is 50MHz.

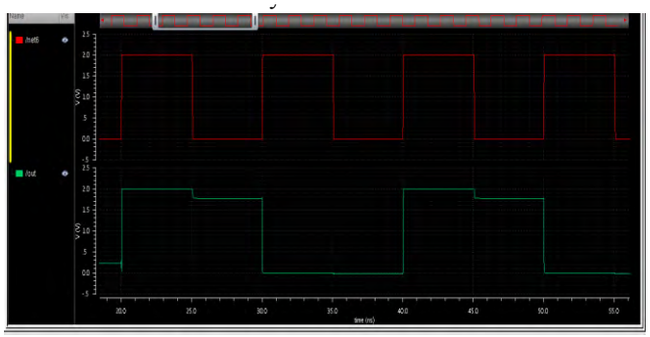

Fig 19: Transient response of Frequency Divider

L. Results of PLL

The below figures show the schematic of PLL, its test bench and various waveforms of PLL in different states i.e. in locked state, unlocked state, and in capture range.

M. Schematic of PLL

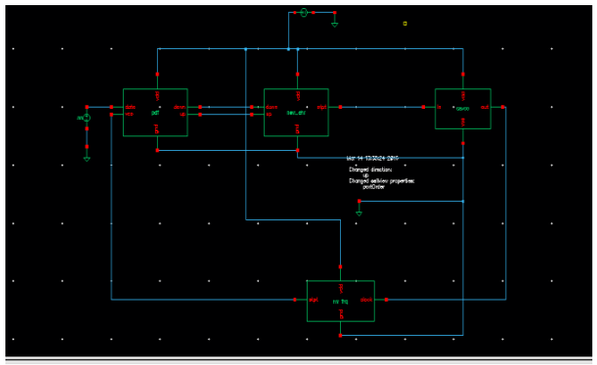

Fig. 20. Schematic diagram of PLL

The schematic of PLL is shown in fig 4.5 contains the four major blocks i.e. phase frequency detector, charge pump/loop filter, voltage controlled oscillator and frequency divider. The below figures show its waveforms.

13. Transient response PLL in unlocked state -Here, the Vout signal is periodic from one-eighth of the Vref signal which means that they both are out of phase and frequency of Vout is also very high. Hence, PLL is in unlocked state. This result is at the 10MHz of Vref signal is shown in fig 21.

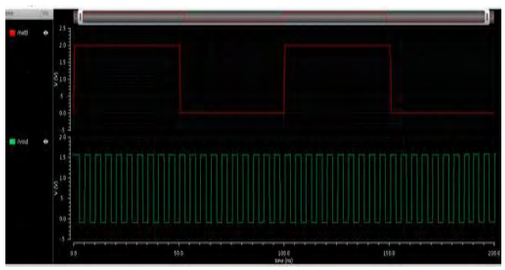

Fig. 21. Response of PLL in unlocked state

N. PLL in locked state- Here, the PLL is in the locked state is shown in fig 22 since the Vout is in perfect synchronization with the Vref signal both in phase and frequency. The result shown below is at the 100MHz of Vref signal.

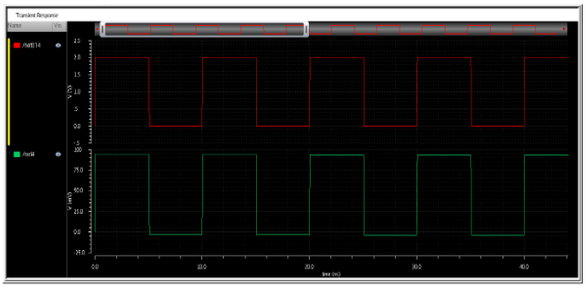

Fig. 22. Response of PLL in locked state

V. Conclusion

In this project, we have designed various blocks of PLL viz. phase frequency detector, charge pump, current starved voltage controlled oscillator, frequency divider which constructed an effective PLL. We have designed a fast locking and low power PLL and simulated using 45 nm CMOS technology through Cadence software. The delay and power dissipation have greatly been reduced by the use of our architecture. Other major parameters have also been greatly improved. Hence, the designed PLL is an energy-efficient PLL thus, enabling us to use it in various applications.

1. In this work a PLL with a very less lock time is presented. The lock time of the PLL is found to be 41.47 ns.
2. The PLL circuit consumes a power of 81.63 uW from a 1.8 V D.C. supply.
3. The lock time of the PLL mainly depends upon the type of PFD architecture used and the parameters of the charge pump and loop filter. So by properly choosing the PFD architecture and adjusting the charge pump current and the loop filter component values a better lock time can be achieved.
4. The center frequency of oscillation of the VCO depends upon the sizing of the transistors. The frequency deviation from the desired value can be reduced by properly choosing the transistor sizes.

Reference

[1] K. K. Abdul Majeed, and B. J. Kailath, “Low power, High Frequency, Free Dead Zone PFD for a PLL Design,” IEEE 2013.

[2] S. Aditya, and S. Moorthi, “A Low Jitter Wide Tuning range Phase Locked Loop with Low Power Consumption in 180nm CMOS Technology,” *Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (Prime Asia),* IEEE 2013.

[3] A. Mishra, G. K. Sharma, and D. Boolchandani, "Performance Analysis of Power Optimal PLL Design Using Five-Stage CS-VCO in 180nm," *International Conference on Signal Propagation and Computer Technology (ICSPCT),* IEEE 2014.

[4] B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill, 2002.

[5.] K. Seung-Hoon, and S.-B. Cho, "Low Phase noise and Fast Locking PLL Frequency Synthesizer for a 915MHz ISM Band", In *Integrated Circuit, ISIC07 International Symposium on,* pp. 592-595, IEEE 2007.

[6] X. Xu, H. Liu, and S. Ao, "Design of low phase noise and fast locking PLL frequency synthesizer," *In International Conference on Electric Information and Control Engineering on,* pp. 4113-4116, 2011.

[7] S. Verma, J. Xu, and T. H. Lee, "A multiply-by-3 coupled ring oscillator for low power frequency synthesis," *IEEE J. Solid State Circuits on*, pp. 709-713, 2004.

[8] G. S. Singh, D. Singh, and S. Moorthi, "Low power low jitter phase locked loop for high speed clock generation," *Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics (PRIMEASIA),* December 2012.

[9] P. Sreehari, P. Devulapalli, D. Kewale, O. Asbe, and K. S. R. Krishna Prasad, "Power Optimized PLL Implementation IN 180nm CMOS Technology," IEEE 2014.

[10] D. Johns, and K. Martin, Analog Integrated Circuits Design (2^{nd} ed.), 1997.

[11] N. H. E. Weste, and K. Eshraghian, "Principles of CMOS VLSI Design: A system Perspective, Addison-Wesley Longman Publishing Co., Inc. Boston, MA.