ISSN.: 2349-7866

Design and Implementation of Multi Stack Voltage Equalizer for Partially Shaded Photo Voltaic Modules using Fuzzy Logic

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Abstract: This paper presents multi stage voltage equalizer to the improvement control performance in PV system to eliminate partial shading issues using fuzzy logic technique. In order to avoid partial shading problem here single switch is used for voltage equalizing purpose then it applied to multi stacked SEPIC converter then get the maximum energy from panels. Here, fuzzy logic concept is used to turn and off for the particular SEPIC switch. Compare to conventional equalizer, these type of single switch topology has minimum size circuits and extract maximum power also. The proposed voltage equalizer can be found by stacking capacitor-inductor-diode (CLD) filter on SEPIC converter. Here, fuzzy logic algorithms are simulated using MATLAB fuzzy logic toolbox. In this paper the fuzzy logic based control circuit is developed to give equal power in all panels. A hardware prototype with three PV panel is implemented. The equalization efficiency is higher than 98% equalization compared with the conventional analog control algorithm. Here, fuzzy logic based multi stack voltage equalizer is simulated using MATLAB/SIMULINK software.

Keywords: Partial shading, Photovoltaic system, SEPIC, Multi stack voltage equalizer, Fuzzy logic.

I. Introduction

In the recent days, PV based power generation has gained more importance due its numerous advantages such as fuel free, requires very little maintenance and environmental benefits. To improve the energy efficiency, it is important to operate PV system always to get at its maximum power. But Partial shading on a photovoltaic (PV) string comprising multiple modules/ substrings triggers issues such as a significant reduction in power generation and the occurrence of multiple maximum power points (MPPs), including global and local MPPs, and various MPPT algorithms. Single-switch voltage equalizers using multi-stacked SEPIC is proposed to settle the partial shading issues. The single-switch topology can considerably simplify the circuits compared with conventional equalizers requiring multiple switches and control techniques are needed.

One of the mail reliability issues of PV systems is the mismatch values between its expected and actual power outputs. This problem can be called PV mismatch. It can have many sources, and the one addressed in this paper is the partial shading of PV modules. Many authors have proposed ideas to mitigate the effects related to partial shading issue.

In photovoltaic (PV) energy systems, PV modules are often connected in series for increased string voltage; however, I-V characteristics mismatches often exist between series connected PV modules, typically as a result of partial shading, manufacturing variability and thermal gradients. Since all modules in a series string share the same current, the overall output power can be limited by underperforming modules. A bypass diode is often connected in parallel with each PV module to mitigate this mismatch and prevent PV hot spotting, but the efficiency loss is still significant when only a central converter is used to perform MPPT on the PV string.

The shaded PV cells will produce less current than the others, which will lead voltage mismatch.

- The other cells impose their current over the shaded cells, making them work under negative voltage, dissipating power and risking destruction.
- The MPPT will track the current of the shaded cells, imposing it over the others and making them produce less energy.

To protect the shaded cells from being destroyed and to minimize losses in power production, PV modules are equipped with bypass diodes. They prevent the shaded cells from working under reverse voltage by short-circuiting them, thus allowing the other cells to work at their normal current [1].

However, bypass diodes deform the *I–V* curves while activated, interfering with the MPPT. This makes the tracking of the MPP impossible for simple algorithms.

II. Single-Switch Voltage Equalizer Using Sepic

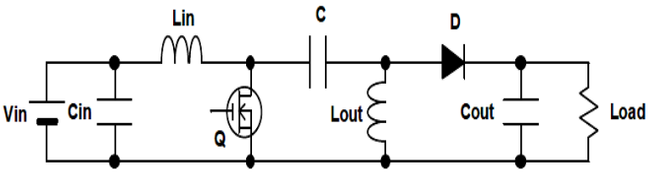


Fig. 1: SEPIC

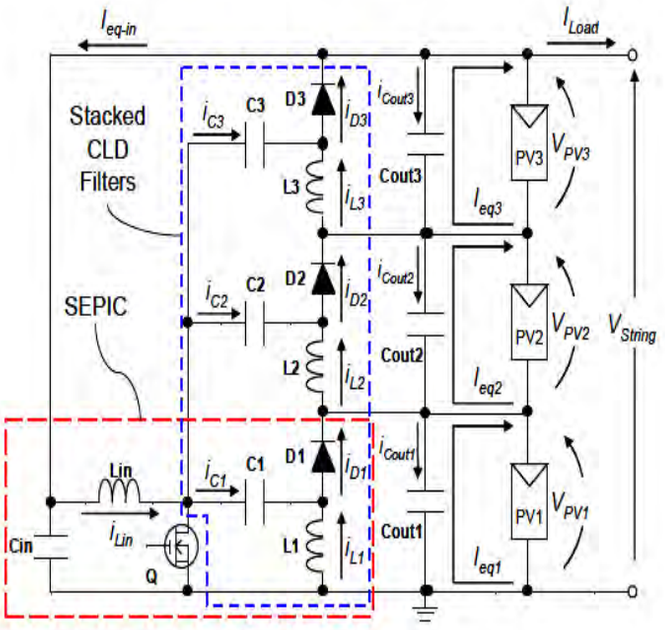


Fig. 2: SEPIC based voltage equalizer

The proposed single-switch voltage equalizers for three PV substrings are shown in the above Fig. 1 and 2. Each PV equalizer is based on one of the buck-boost converters with stacked CLD filters. In all proposed equalizer topologies, an asymmetric square-wave voltage is produced across the switch Q and capacitors C1–C3 act as coupling capacitors, allowing only the ac component to flow through. Although the stacked CLD filters have different dc voltage levels, the same asymmetric square voltage wave is applied to all inductors L1–L3 due to the ac coupling, producing a uniform output voltage for each PV substring.

III. Circuit Analysis

The proposed single-switch voltage equalizers for three PV substrings are shown in Fig. 2. The PV equalizer is based on buck-boost converter (SEPIC) with stacked CLD filters and its produce an asymmetric square-wave voltage across the switch Q, and capacitors C_1–C_3 act as coupling capacitors, allowing only the ac component to flow through. Although the stacked CLD filters have different dc voltage levels, the same asymmetric square voltage wave is applied to all inductors L_1–L_3 due to the ac coupling, producing a uniform output voltage for each PV substring.

Based on Kirchhoff's current law in Fig. 3, the average current of L_i, I_{Li}, equates to that of Di, I_{Di}, because the average current of Ci must be zero under a steady-state condition. the equalization current supplied to PVi, I*eq-i* is

$$I_{eq\text{-}I} = I_{Li} = I_{Di} \quad (1)$$

Therefore, both I_{L1}–I_{L3} and I_{D1}–I_{D3} are dependent on partial-shading conditions.

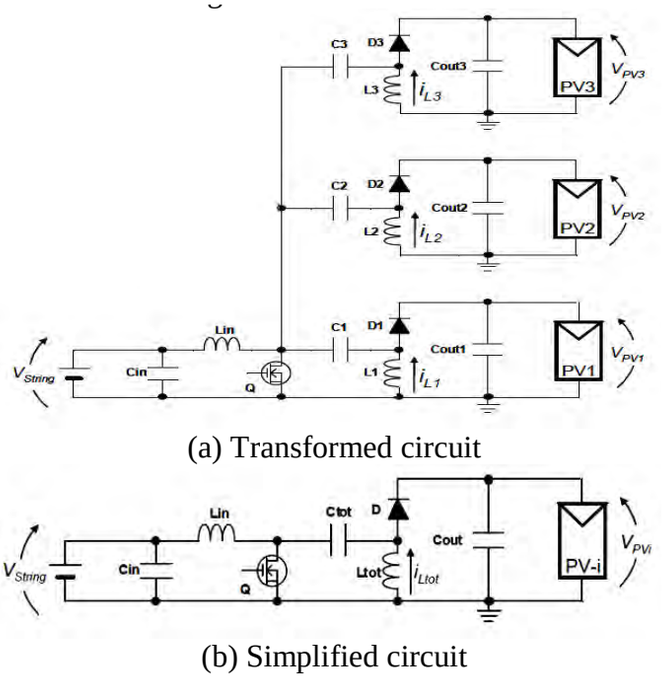


Fig. 3 (a) Transformed and (b) Simplified circuits of the SEPIC-based voltage equalizer

As mentioned in Section III, thanks to the ac coupling of C1–C3, all inductors of L1–L3 are driven by the same asymmetric square-wave voltage, although the stacked CLD filters are at different dc voltage levels. Since the stacked CLD filters are ac-coupled, the series-connected substrings can be equivalently separated and grounded as shown in Fig. 3 (a), in which a dc voltage source with V_{String} that is equivalent to the sum of V_{PV1}–V_{PV3} is used to power the equalizer. In this transformed voltage equalizer, both the CLD filters and PV1–PV3 are connected in parallel. Accordingly, the transformed circuit shown in Fig. 3 (a) can be simplified to the equivalent circuit shown in Fig. 3 (b), which is identical to a traditional SEPIC shown in Fig. 2. This allows the overall operation of the proposed voltage equalizer to be analyzed and expressed [2].

In the simplified equivalent circuit, the current of L_{tot}, i_{Ltot}, equates to the sum of i_{L1}–i_{L3};

$$i_{Ltot} = i_{L1} + i_{L2} + i_{L3} \quad (2)$$

the total of I_{eq1}–I_{eq3}, $I_{eq\text{-}tot}$, is

$$I_{eq\text{-}tot} = I_{eq1+} I_{eq2+} I_{eq3} \quad (3)$$

Since all inductors in the CLD filters are driven by the same asymmetric square-wave voltage of *vL*, the inductance of L_{tot} in the simplified circuit, L_{tot}, is yielded as

$$L_{tot} = V_L(dt/di_{L1} + dt/di_{L2} + dt/di_{L3}) \quad (4)$$

$$L_{tot} = L_i/3 \quad (5)$$

where *Li* is the inductance of L_1–L_3. Capacitors C_1–C_3 and C_{out1}–C_{out3}, respectively, are virtually connected in parallel, and therefore, the capacitances of C_{tot} and C_{out} in the simplified circuit, C_{tot} and C_{out}, are

$$C_{tot} = 3C_i\,,\ C_{out} = 3C_{out\text{-}i} \quad (6)$$

where C_i and $C_{out\text{-}i}$, respectively, are the capacitances of C_1–C_3 and C_{out1}–C_{out3} [3].

IV. Modes of Operation

The proposed voltage equalizers operate either in continuous conduction mode (CCM) or discontinuous conduction mode (DCM), similar to traditional buck-boost converters. The open-loop operation in DCM is no longer advantageous, and the CCM operation is considered desirable from the perspective of current rating of components. The operational analysis of continuous and discontinuous operation modes are explained using the original circuit shown Fig. 4 (a), while mathematical analyses will be performed and equations developed for the simplified circuit.

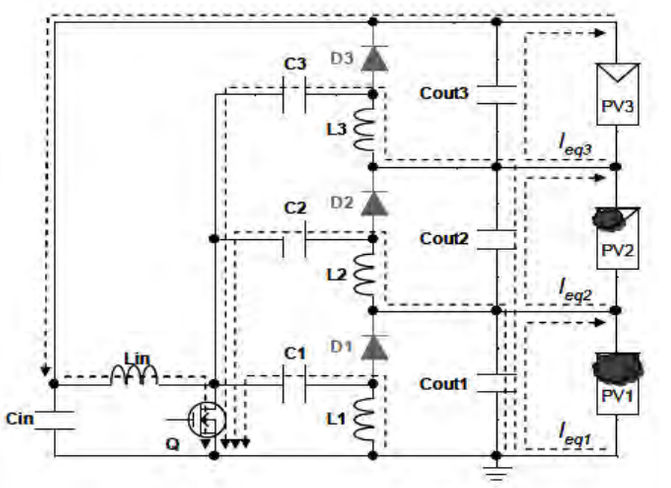
The key operation waveforms and current flow paths in DCM and CCM under the partially shaded condition are shown in Fig. 5 and 6, respectively.

A. DCM Operation

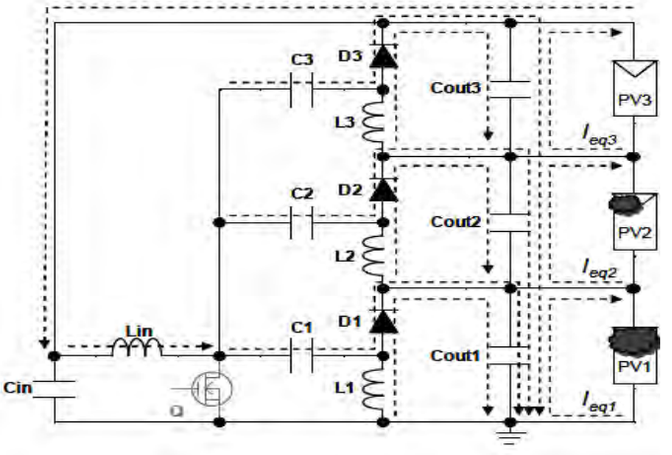
During the on period, T_{on}, all inductor currents, i_{Lin} and i_{Li}, linearly increase and flow through the switch Q. i_{L1}–i_{L3} flow through C_1–C_3 and C_{out1}–C_{out2}. The lower the position of C_{out1}–C_{out3}, the higher the current tends to flow; the current of C_{out1}, i_{Cout1}, shows the largest amplitude. For example, i_{L2} only flows through C_{out1}, whereas i_{L3} flows through both C_{out1} and C_{out2}. Thus, currents flowing through the upper smoothing capacitors are superimposed on lower ones.

As Q is turned off, the operation moves to $T_{off\text{-}a}$ period. Diodes D_1–D_3 start conducting, and the inductor current linearly [4] declines.

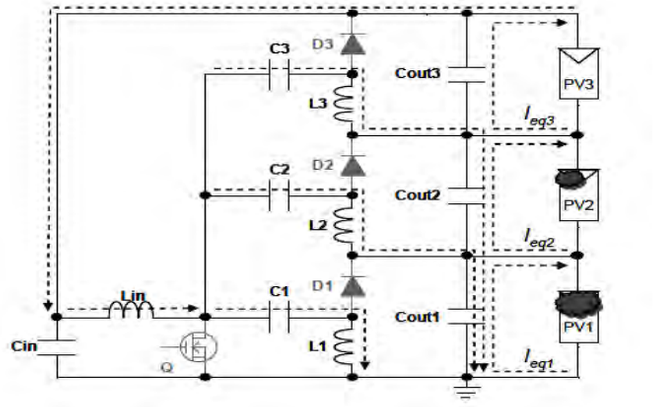
Energies stored in L_1–L_3 in the previous T_{on} period are discharged to respective smoothing capacitors in this mode. i_{Lin} is distributed to C_1-D_1–C_3-D_3 branches and flows toward C_{out1}–C_{out3}. Depending on the shading conditions, some diodes that correspond to slightly-shaded or unshaded substrings cease to conduct sooner than the others.



(a) T_{on} period



(b) $T_{off\text{-}a}$ period



(c) $T_{off\text{-}b}$ period (for DCM only)

Fig. 4: Current flow paths in period of (a) T_{on}, (b) $T_{off\text{-}a}$, (c) $T_{off\text{-}b}$, (for CCM only)

The $T_{off\text{-}b}$ period begins as all diodes cease. Since the applied voltages of all inductors in this period are zero, all currents, including iC_i, remain constant. The duty cycle of $T_{off\text{-}a}$ period, D_a, is given by

$$D_a = DV_{string} / (V_{PVi} + V_D) \quad (7)$$

where D is the duty cycle of Q, and V_D is the forward voltage drop of the diodes.

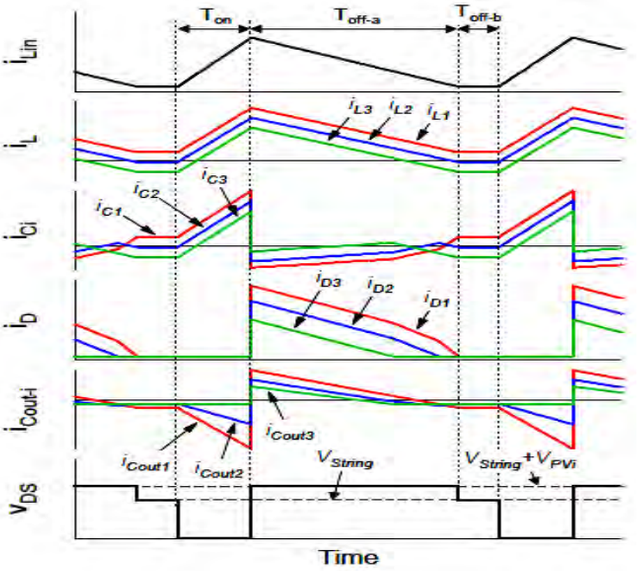


Fig. 5: Key operation waveforms in DCM

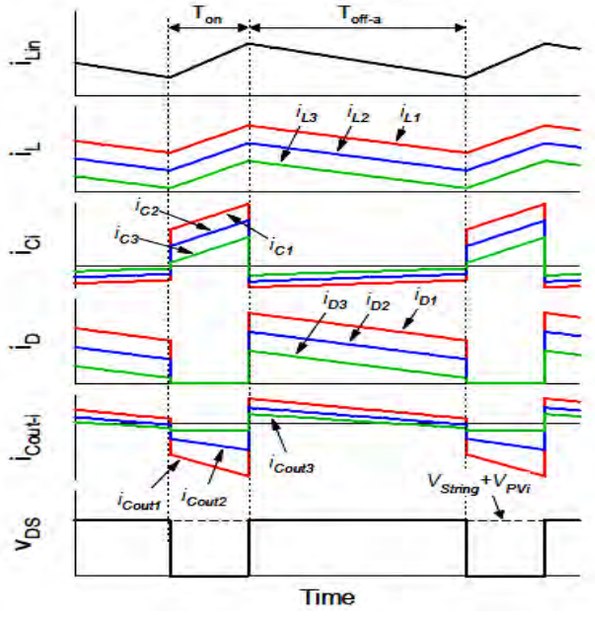


Fig. 6: Key operation waveforms in CCM

B. CCM Operation

The operational waveforms in CCM are shown in Fig. 7. The voltage conversion ratio and current relationship in CCM are given by

$$V_{PV} = \frac{D}{1-D_{string}} V \quad (8)$$

$$I_{string} = \frac{D}{1-D} I_{in} \quad (9)$$

C. Component Rating

a) Inductors:

Similar to ordinary converters, inductance values of *Li* and *Lin* should be designed considering a full load condition. The full load condition occurs when one substring in unshaded while the rest two substrings are completely shaded; each shaded substring produces no power but requires as much power as the unshaded one produces. Thus, in terms of a processed power, the full load condition is considered as the worst shading condition. Ripple ratios of I_{Li} and I_{Lin}, α_{Li} and α_{Lin}, are defined as

$$\left\{ \begin{array}{l} \alpha_{Li} = \dfrac{\Delta I_{Li}}{I_{ti}} = \dfrac{V_{string} D T_s}{L_i I_{eq-i}} \\ \alpha_{Lin} = \dfrac{\Delta I_{Lin}}{I_{tin}} = \dfrac{V_{string}(1-D)}{L_{in} I_{eq-in}} \end{array} \right\} \quad (10)$$

where ΔI_{Li} and ΔI_{Lin} are the ripple currents of L_i and L_{in}. Although these values vary depending on shading conditions, $\alpha L_i = \alpha L_{in}$ for the worst shading case is deemed a reasonable design [5]. The worst shading condition occurs when two substrings are fully shaded, and therefore,

$$L_i / L_{in} = D/(1\text{-}D)(I_{eq\text{-}tot}/I_{eq\text{-}i}) \approx 2/3 \quad (11)$$

b) Capacitors (C_1–C_3):

Since the substring voltages are equalized as $V_{PVi} = V_{String}/3$, the voltages of C_1–C_3, V_{C1}–V_{C3}, are

$$V_{c1} = V_{String}, V_{c2} = 2/3V_{String}, V_{c3} = 1/3V_{String} \quad (12)$$

$$I_{Rms} = I_{Li}\sqrt{\frac{D}{1-D}}$$

c) Smoothing Capacitors (C_{out1}–C_{out3}):

The RMS current rating of $C_{out\text{-}i}$ needs to be determined considering each capacitor position because of the current superposition, as Currents from the stacked CLD filters are buffered by $C_{out\text{-}i}$, while $C_{out\text{-}i}$ supplies an equalization current of $I_{eq\text{-}i}$ for PV_i. The current of C_{out1}, i_{Cout1}, is expressed as

V. Design of Fuzzy Logic Controller

The numerical input of the solar panel voltage V is also converted into two sets of fuzzy variables, i.e., $\mu_{eq;V}$ and $\mu_{st;V}$. For example, $\mu eq;\Delta V = Fuzeq(\Delta V) = 1$ and $\mu st;\Delta V = Fuzst(\Delta V) = 0.5$ are the fuzzy results from ΔV when $0.1\ V < \Delta V < 0.3\ V$. The linguistic control values are achieved based on the input fuzzy variables and the pre-constructed rule bases in the inference engine which is shown in Fig. 7. A multiplying inference engine is adopted, i.e.,

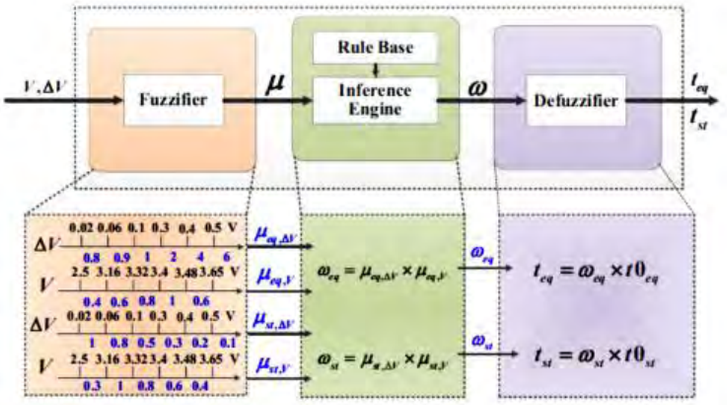


Fig. 7: Block diagram of the fuzzy logic controller

$$\begin{aligned} i_{cout1} &= \{-\left(i_{c2}+i_{c3}\right)-I_{eq1} \\ &= -\left(I_{l1}+I_{l2}+I_{l3}\right):T_{on} \end{aligned} \tag{13}$$

where *t*0*eq* and *t*0*st* are the nominal equalization time and the nominal standing time, respectively [6].

VI. Simulation Results and Discussion

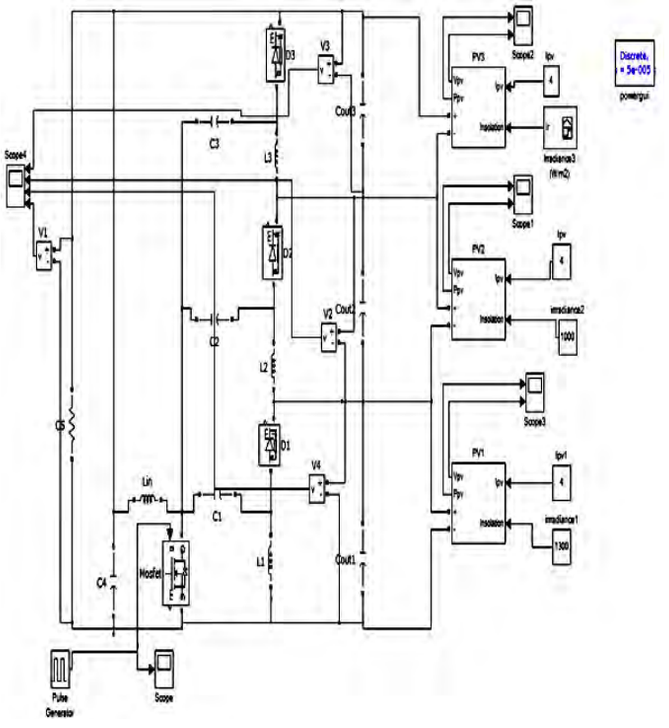


Fig. 8: Simulation diagram of fuzzy based multi-stack voltage equalizer

Fig. 8 shows simulation diagram and In order to valiadate the performance of the above equalizer a simulation model was designed in matlab-simulink targeting a 100-W PV panel consisting of three sub panels each with typical operating voltage range of 10–24 V. The proposed equalizer is validated under three different scnearious with the parameters listed in the Table 1 [7].

The proposed equalizer is validated among three conditions which are listed below:

- *Case 1*: normal mode all on equal voltage balancing [8].
- *Case 2*: Panel 1 with shaded and panel 2 and 3 are in normal condition [9].

Table I: Paramerters Used in the Proposed Circuit Equalizer

Components	Rating
Equalizer Capacitors	C_1-C_3-40μF
Output capacitors	150 μF
Inductors – Equalizer	68 μH
Lout	86 μH
Cin	1000 μF
Solar panels-3	12-20 volts 17.4 $V_{max\text{-}mpp}$

A. Case 1:

Input is around 19.4 volts as common for all the panels and the output boost voltage is at 44V represents the boost mode operation of the proposed converter on ideal mode. Which is shown in Fig. 9.

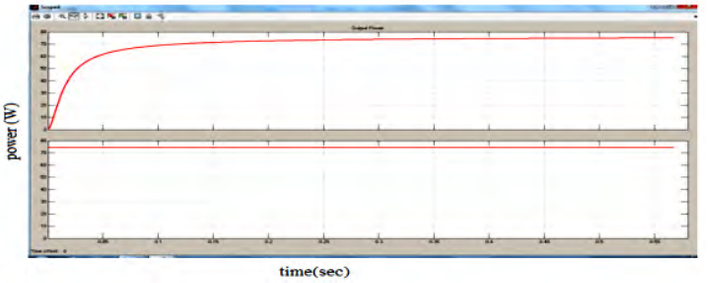


Fig. 9: The input and out power chrecteristcis of the converter

B. Case 2:

In this mode equalization pattern of the proposed equalizer is studied by changing the irradiation of the solar panel, which makes the panel as partial shading, panel 1 is partially shaded and the voltage compensation is done by adjusting the duty ratio according to the voltage variations of the panel.

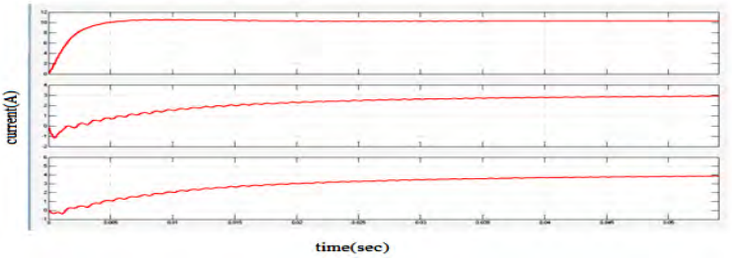


Fig. 10: Compensation current of PV panel

Fig. 10, shows compensational curerent of PV panel, Here variations from initially panel 1 statrs to compensate which inturn raises the compensation current and maintian the stability of the converter.

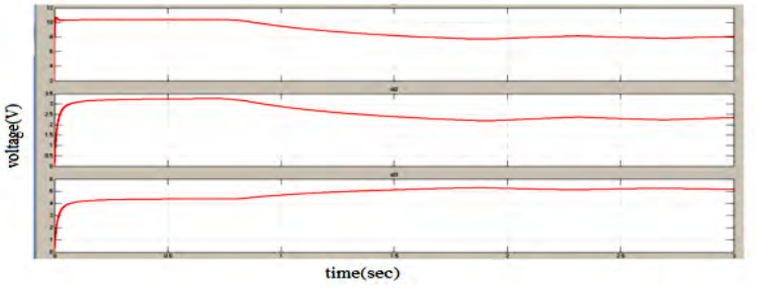


Fig. 11: Compensation capacitor voltages of PV panel

In Fig. 11 shows the compensation voltage prodcued by the panels due to the control intiation intially panel 1 starts to compenste until the voltage variations starts to change the compensations currrnewt after 0.75 sec panel 1 starts to devrease and panel 2 and 3 starts to compensate by providing current by regulating voltage, X axis in time and Y axis in current.

In Fig. 12 shows the current vairations that changes the compensation current behaviour which is compensated by other panels during thevarious time intervals, the deviation of power is been compensated by the panels, X axis in time and Y axis in current.

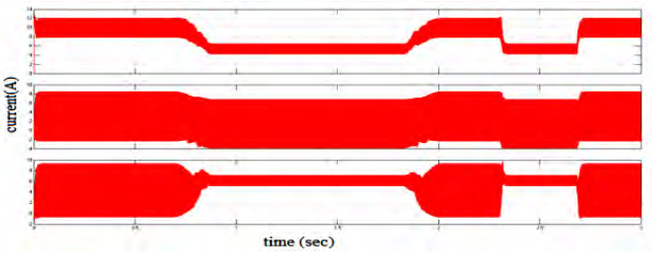


Fig. 12: Capacitor C_{out} currents

VII. Fuzzy Simulation Reults

In order to compensate the ripple current variations in the PV panel circuit ,the fuzzy logic controller is used and the results are shown in below Fig. 13. After framing the rules defuzzificztion method is also applied to convert fuzzy to crisp.

Fig. 13: The fuzzy rules

VIII. Conclusion

In this project, the proposed voltage equalizers can be derived by stacking CLD filters on the traditional converter topologies, the proposed structure of the converter is simpler and easier to implement, the proposed fuzzy based equalization strategy based on the fuzzy logic controller has better voltage regulation characteristics under partial shading conditions, the Fuzzy controller provides the necessary controller action to control the voltage equalizers to supply excessive equalization currents from the unshaded panels for shaded substrings, which unturn needlessly increasing power conversion loss.

The proposed fuzzy based equalization technique provides a better compensation over the conventional equalizers which is light weight in algorithm can be implemented towards a simpler hardware. The extractable maximum powers with equalization were considerably increased compared with those without equalization, demonstrating the efficiency of the proposed voltage equalizer.

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