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A Review on Design of Full Adder Circuit Using Shannon Modified Method

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Abstract: In this paper, an 8 bit high speed full adder is designed based on Shannon's expansion. This adder is implemented by using CMOS process technology. The proposed adder provides compromise both cost and performance in carry propagation adder design. Since, in parallel adder the carry suffer from the propagation delay. As the adder block increases the propagation delay also increased. So to provide constant amount of propagation delay into the adder, look ahead carry adder design and to enhance the performance of this design Shannon's expansion is used. It also reduced the computational time. So it will be faster than any other adder design.

Keywords: ALU, CMOS technology, Look ahead carry, Propagation delay, Shannon's expansion.

I. Introduction

The adder is one of the most critical components of a processor, as it is used in the Arithmetic Logic Unit (ALU), in the floating-point unit and for address generation in case of cache or memory access. The arithmetic operation such as, addition and subtraction used in VLSI design have their special significance. Almost all the applications required these operations; with increasing demand for mobile electronic devices such as cellular phones and laptop computers which requires power efficient VLSI circuits. Since these requirement increases day by day, Leakage power plays a vital role in current CMOS technologies [3]. As feature size shrinks leakage power also increasing. Power dissipation becomes as important consideration as performance and area for chip design in present days VLSI industry. So the adder should be designed in such a way that it should have high speed of operations, less power consumption. An adder is a circuit which performs the addition of digital numbers. Many computers and processors use arithmetic logics in the form of adders [5]. There are various number formats in which this adder can be designed, Numerical representations such as binary coded decimalor excess-3. The most essential logic elements are binary numbers in a digital system than other Arithmetic units (ALU), such as multipliers, dividers etc. any improvement in the binary addition will improve the system performance. We use Karnaugh map, to reduce the variables and also to minimize solution [2]. In this paper, we use Shannon's method and also compare the performance in terms of power dissipation, delay and area.

A. Objective

Shannon's expansion based an efficient high-speed 8-bit full adder is designed. This proposed adder provides better performance in carry propagation adder design with low cost. It increases the speed by decreasing the computational time.

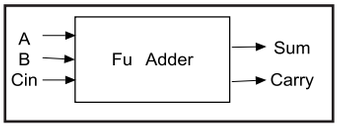

Fig. 1: Block Diagram of Full Adder

Table I: Truth Table of Full Adder

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$Sum = A \oplus B \oplus C_{in}$$

$$Carry = (A+B)\ C\ +\ (A\ B)$$

II. Shannon Theorem

Now, The Shannon Theorem can be written as the many variables function, $f(b_0, b_1, b_2, y, b_i, y, b_n)$ it can be written as the sum of two terms i.e. one with a specific variable ai, set to 0, and one with it set to1.

$$f(b_0, b_1, b_2, \cdots, b_i, \cdots, y, b_n) = \bar{b}_i\, f(b_0, b_1, b_2, \cdots 0, \cdots, y, b_n) + b_i f(b_0, b_1, b_2, \cdots 1, \cdots, y, b_n)$$

n-1 variables are used as control inputs along with 3 data lines which is set to '1' when the Shannon theorem is applied to any logical function and the source are connected to the biasing pin i.e. VDD and VDD is further connected to logic '0'.

III. Existing Methods

A. Multiplexing Control Input Technique (MCIT)

MCIT technique is completely based on the Karnaugh map [3]. From the truth table of full adder the following theBoolean expressions are derived for the sum and carry. These expressions are:

$$Carry = AB + BC + CA$$

$$Sum = ABC + \bar{A}\bar{B}C + A\bar{B}\bar{C} + \bar{A}B\bar{C}$$

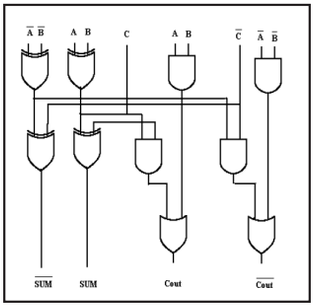

Fig. 2: MCIT for a Full Adder Circuit Using Logic Gates

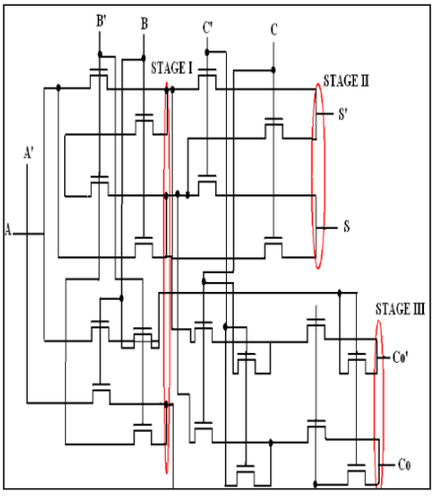

Fig. 3: MCIT for a Full Adder Circuit Using Pass Transistor

B. Existing Shannon Based Full Adder Cell

This architecture is formed by combining MCIT and Shannon operation together to obtained sum and Carry respectively [4].

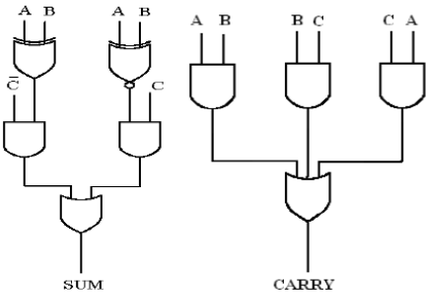

Fig. 4: Shannon Based Full Adder Using Logic Gates

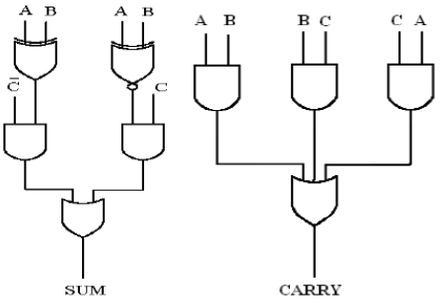

Fig. 5: Shannon Based Full Adder Using Pass Transistor Logic

C. Look Ahead Carry Adder Method

A Look ahead carry adder is a much faster parallel adder than any other ordinary parallel adder but since it reduces the propagation delay it requires more number of gates that makes the circuit more complex and costly. In this design, the logic at carry over fixed groups of bits of the adder is reduced to two-level logic, which is the transformation of the ripple carry design.

The complete circuits which are shown in Fig. 8. The propagation delay of this adder is fixed to $4t_{pd}$ only. As the number of bits increased, the propagation delay remains fixed.

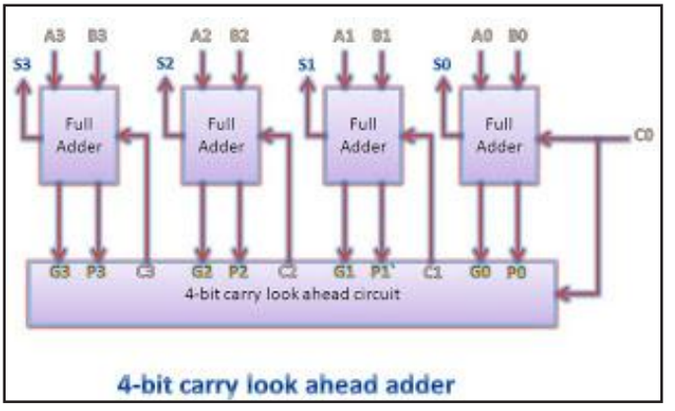

Fig. 6: Block Diagram of Look Ahead Carry

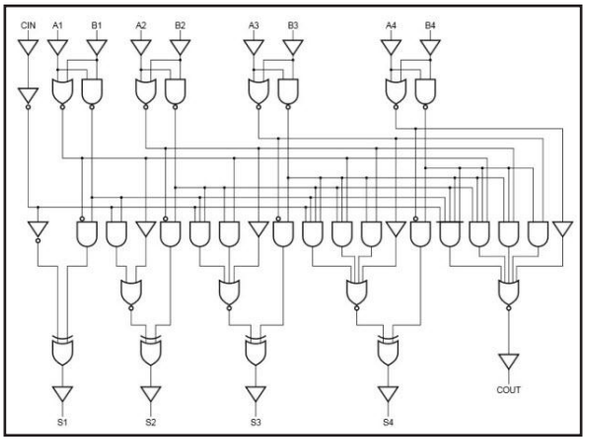

Fig. 7: Internal Circuit of Look Ahead Circuit

D. Proposed Shannon Based Full Adder Cell

To obtain the proposed Shannon based full adder expression for the carry, some change has to be done with the actual adder circuit and expressions. Condensed form of sum and carry are obtained with the Shannon's theorem. Since, the required transistors get reduced. There are six transistor are present to obtained carry expression in the existing design method which makes circuit little bit complex whereas in the proposed full adder design method only two transistors will be used. Thus, number of transistor in this design gets reduced the area required to design the circuit gets minimized and also the power reduced to considerable amount.

E. Proposed Shannon's Theorem

The modified expression for the proposed method is:

$$Carry = (A \oplus B)\mathrm{B} + (A \oplus B)C)$$

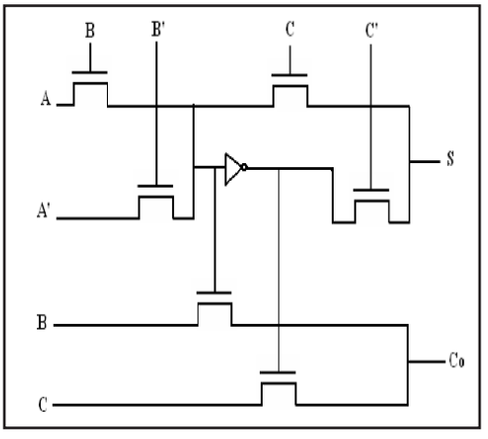

Fig. 8: Proposed Shannon Based Full Adder Using Pass Transistor Logic

F. Half Adder

$$Sum = A \oplus B$$
$$Carry = A\ B$$

G. Full Adder

$$Sum = A \oplus B \oplus C$$
$$Carry = \ (A + B)C \ + \ (A\ B)$$

IV. Conclusion

The proposed Shannon based full adder architecture will give better result and due to area requirement by the transistor get reduced, the power consumption also reduced. This proposed method is much better approach than the existing method to design full adder circuit.

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